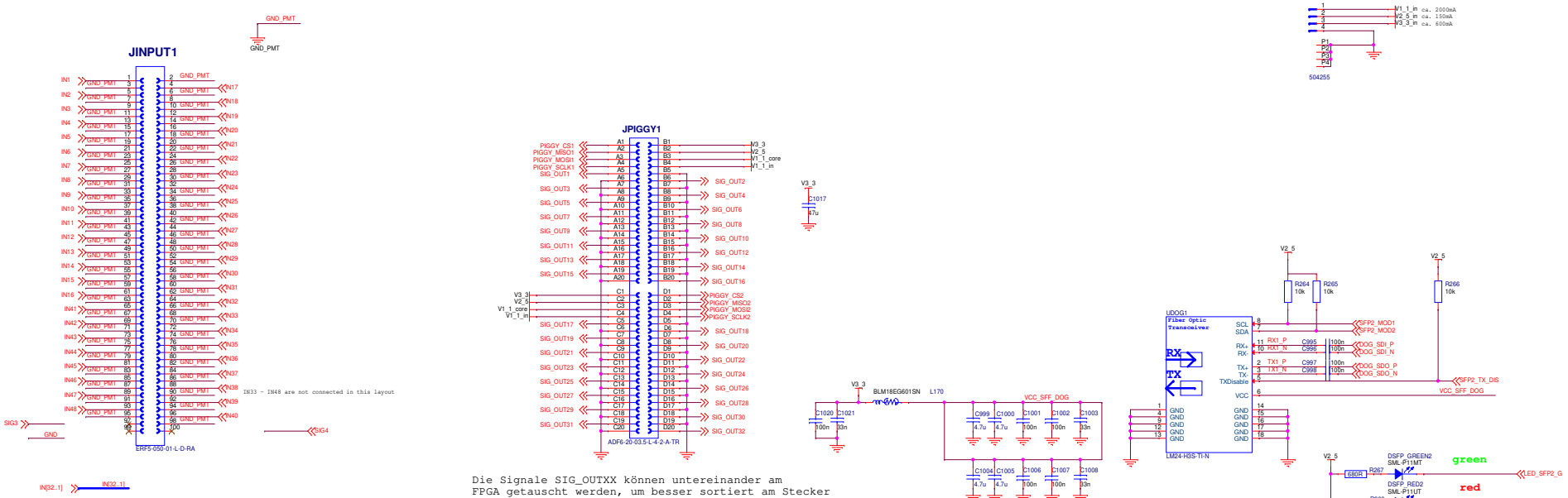

Die Signale SIG_OUTXX können untereinander am FPGA getauscht werden, um besser sortiert am Stecker JPIGGY1 anzukommen.

Die Signale PIGGY_XXX können untereinander am FPGA getauscht werden, um besser sortiert am Stecker JPIGGY1 anzukommen.

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I/O Connectors	
Design: K:\GSU\OBC\OME_AND_KISS\DIRICH\DIRICH502\DIRICH502.DSN	
Modified: Wednesday, February 28, 2024	Size: A2 Page: 1 / 9
Designer: M.Traxler / H. Heggen	Layouter: H.Kayan

PWM_IN[32..1]

PWM_IN[32..1]

PWM_IN:
these are outputs from this FPGAs point of view....

UDAC1-2

PWM_IN8 H9 PB4A_2_CSSPIN_T
PWM_IN12 J8 PB4B_2_C
H8 PB7A_2_T
G7 PB7B_2_C
H7 PB9A_2_MCLK/CCLK_T
PWM_IN3 J7 PB9B_2_SO/SPISO_C
PWM_IN13 J6 PB13A_2_PCLKT2_0_T
H6 PB13B_2_PCLKC2_0_C
H5 PB15A_2_T
PWM_IN14 J5 PB15B_2_C
G4 PB20A_2_PCLKT2_1_T
H4 PB20B_2_PCLKC2_1_C
G3 PB23A_2_T
G2 PB23B_2_C
H3 PB24A_2_T
PWM_IN2 J3 PB24B_2_C
H2 PB27A_2_T
PWM_IN15 J2 PB27B_2_C
G1 PB30A_2_SN_T
PWM_IN16 H1 PB30B_2_SI/SISPI_C
PWM_IN11 B9 PL4A_5_L_GPLLT_IN_T
C8 PL4B_5_L_GPLLC_IN_C
D8 PL5A_5_T
E6 PL7A_5_T
E7 PL7B_5_C
DAC1_CTRL2 D9 PL8C_5_T
E8 PL8D_5_C
F8 PL15A_3_T
F7 PL15B_3_C
DAC1_CTRL3 F6 PL16A_3_T
G9 PL17A_3_PCLKT3_0_T
G8 PL17B_3_PCLKC3_0_C
F5 PL18A_3_T
F4 PL18B_3_C
D7 PT9A_0_T_TLVDS
D6 PT9B_0_C_TLVDS
D5 PT10A_0_T_TLVDS
C6 PT10B_0_C_TLVDS
PWM_IN6 A8 PT11A_0_T_TLVDS
B8 PT11B_0_C_TLVDS
PWM_IN10 A6 PT18A_0_PCLKT0_1_T_TLVDS
B6 PT18B_0_PCLKC0_1_C_TLVDS
E3 PT19A_0_T_TLVDS
D3 PT19B_0_C_TLVDS
A5 PT20C_0_SCL/PCLKT0_0_T
DAC1_SCL B5 PT20D_0_SDA/PCLKC0_0_C
DAC1_SDA C3 PT21A_0_T_TLVDS
PWM_IN9 B4 PT21B_0_C_TLVDS
F2 PT22A_0_T_TLVDS
E2 PT22B_0_C_TLVDS
R231 0R C2 PT23D_0_PROGRAMN_C
B3 PT24A_0_T_TLVDS
PWM_IN7 A3 PT24B_0_C_TLVDS
F1 PT25A_0_T_TLVDS
DAC1_CTRL1 E1 PT25B_0_C_TLVDS
DAC1_CTRL0 PWM_IN5 A2 PT27A_0_T_TLVDS
B2 PT27B_0_C_TLVDS
PWM_IN1 C1 PT28C_0_INITN_T
PWM_IN4 B1 PT28D_0_DONE_C

LCMXO3LF-4300E-5UWG81CTR50

GND

UDAC2-2

PWM_IN22 H9 PB4A_2_CSSPIN_T
PWM_IN25 J8 PB4B_2_C
H8 PB7A_2_T
G7 PB7B_2_C
H7 PB9A_2_MCLK/CCLK_T
PWM_IN24 J7 PB9B_2_SO/SPISO_C
PWM_IN30 J6 PB13A_2_PCLKT2_0_T
H6 PB13B_2_PCLKC2_0_C
H5 PB15A_2_T
PWM_IN28 J5 PB15B_2_C
G4 PB20A_2_PCLKT2_1_T
H4 PB20B_2_PCLKC2_1_C
G3 PB23A_2_T
G2 PB23B_2_C
H3 PB24A_2_T
PWM_IN29 J3 PB24B_2_C
H2 PB27A_2_T
PWM_IN26 J2 PB27B_2_C
For identification of the FPGA G1 PB30A_2_SN_T
PWM_IN27 H1 PB30B_2_SI/SISPI_C
PWM_IN23 B9 PL4A_5_L_GPLLT_IN_T
C8 PL4B_5_L_GPLLC_IN_C
D8 PL5A_5_T
E6 PL7A_5_T
E7 PL7B_5_C
DAC2_CTRL2 D9 PL8C_5_T
E8 PL8D_5_C
F8 PL15A_3_T
F7 PL15B_3_C
DAC2_CTRL3 F6 PL16A_3_T
G9 PL17A_3_PCLKT3_0_T
G8 PL17B_3_PCLKC3_0_C
F5 PL18A_3_T
F4 PL18B_3_C
D7 PT9A_0_T_TLVDS
D6 PT9B_0_C_TLVDS
D5 PT10A_0_T_TLVDS
C6 PT10B_0_C_TLVDS
PWM_IN20 A8 PT11A_0_T_TLVDS
B8 PT11B_0_C_TLVDS
PWM_IN17 A6 PT18A_0_PCLKT0_1_T_TLVDS
B6 PT18B_0_PCLKC0_1_C_TLVDS
E3 PT19A_0_T_TLVDS
D3 PT19B_0_C_TLVDS
A5 PT20C_0_SCL/PCLKT0_0_T
DAC2_SCL B5 PT20D_0_SDA/PCLKC0_0_C
DAC2_SDA C3 PT21A_0_T_TLVDS
PWM_IN18 B4 PT21B_0_C_TLVDS
F2 PT22A_0_T_TLVDS
E2 PT22B_0_C_TLVDS
R232 0R C2 PT23D_0_PROGRAMN_C
B3 PT24A_0_T_TLVDS
PWM_IN19 A3 PT24B_0_C_TLVDS
F1 PT25A_0_T_TLVDS
DAC2_CTRL1 E1 PT25B_0_C_TLVDS
DAC2_CTRL0 PWM_IN32 A2 PT27A_0_T_TLVDS
B2 PT27B_0_C_TLVDS
PWM_IN31 C1 PT28C_0_INITN_T
PWM_IN21 B1 PT28D_0_DONE_C

LCMXO3LF-4300E-5UWG81CTR50

GND

UDAC1-1

GND A1 GND_0
A9 GND_1
E5 GND_2
G5 GND_3
J1 GND_4
J9 GND_5
V1_1_core C4 VCC_0
D1 VCC_1
F3 VCC_2
E9 VCC_3
V2_5 A4 VCCIO0_0
C5 VCCIO0_1
C7 VCCIO0_2
G6 VCCIO2_0
J4 VCCIO2_1
F9 VCCIO3_0
C9 VCCIO5_0

LCMXO3LF-4300E-5UWG81CTR50

UDAC2-1

GND A1 GND_0
A9 GND_1
E5 GND_2
G5 GND_3
J1 GND_4
J9 GND_5
V1_1_core C4 VCC_0
D1 VCC_1
F3 VCC_2
E9 VCC_3
V2_5 A4 VCCIO0_0
C5 VCCIO0_1
C7 VCCIO0_2
G6 VCCIO2_0
J4 VCCIO2_1
F9 VCCIO3_0
C9 VCCIO5_0

LCMXO3LF-4300E-5UWG81CTR50

UDAC1-3

FDAC_JTAG_TCK
FDAC_JTAG_TMS
FDAC1_JTAG_TDI B7 PT13C_0_TDO_T
A7 PT13D_0_TDI_C
E4 PT15C_0_TCK_T
D4 PT15D_0_TMS_C
D2 PT23C_0_JTAGENB_T

LCMXO3LF-4300E-5UWG81CTR50

UDAC2-3

FDAC2_JTAG_TDO B7 PT13C_0_TDO_T
A7 PT13D_0_TDI_C
E4 PT15C_0_TCK_T
D4 PT15D_0_TMS_C
D2 PT23C_0_JTAGENB_T

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V2_5

C650 C651 C652 C653 C654 C655 C658 C659 C660 C661 C662 C663 C664 C665 C666 C667 C668 C669
4.7u 4.7u 4.7u 4.7u 4.7u 4.7u 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n

C677 C678 C679 C680 C681 C682 C683 C684 C685 C686 C687 C688 C689 C690 C693 C694 C695 C696
47n 47n 47n 47n 47n 47n 47n 47n 47n 47n 10n 10n 10n 10n 10n 10n 10n 10n

V1_1_core

C606 C607 C608 C609 C610 C698 C699 C700 C701 C702 C703 C704 C705 C706 C707 C708 C709
4.7u 4.7u 4.7u 4.7u 4.7u 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n

C711 C712 C713 C714 C715 C716 C717 C718 C719 C720 C721 C722 C723 C724 C725 C726 C727 C728 C729 C730
47n 47n 47n 47n 47n 47n 47n 47n 47n 47n 10n 10n 10n 10n 10n 10n 10n 10n 10n 10n

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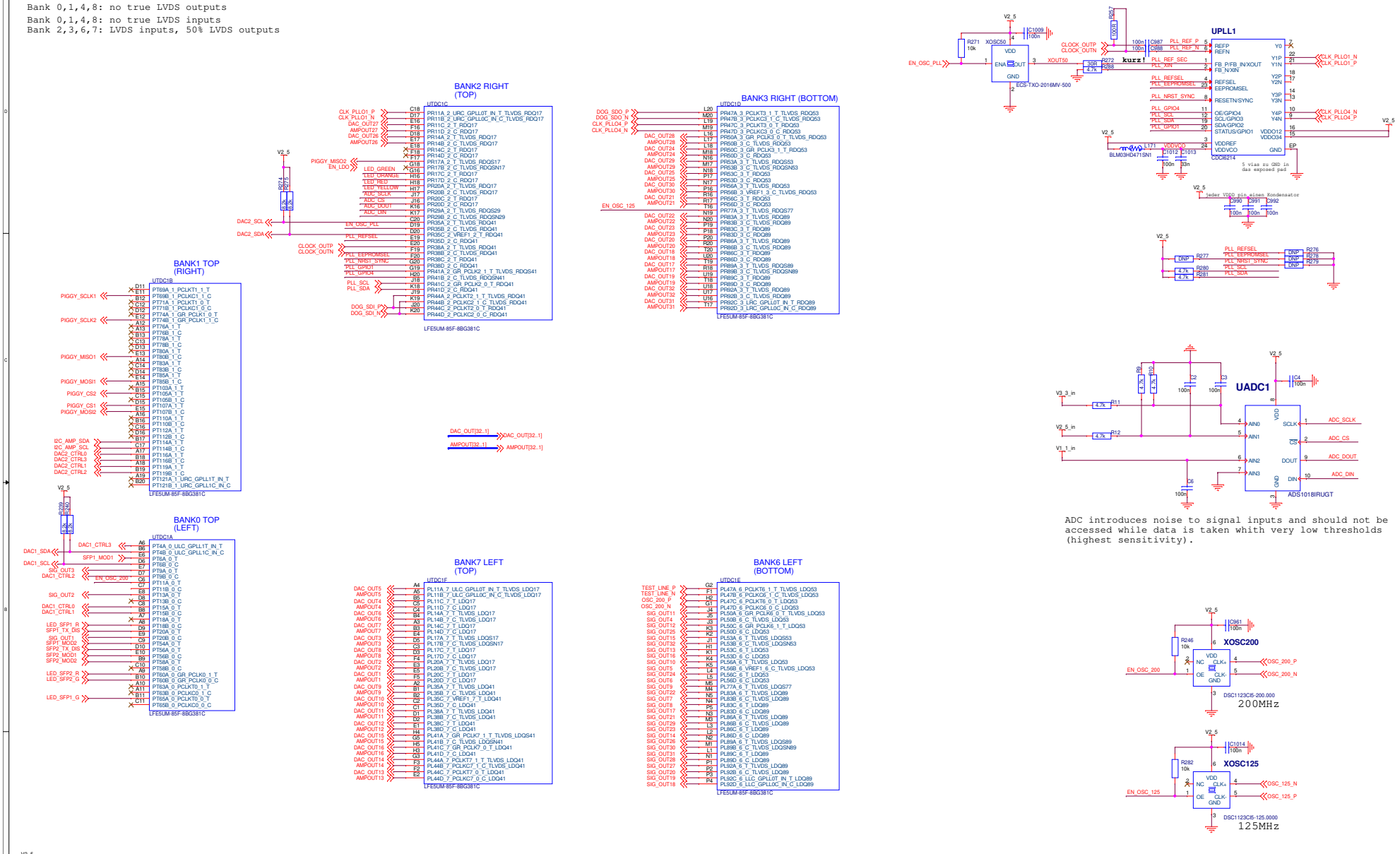
DAC_FPGA

Design:	K:\GSI\OB\COME_AND_KISS\DIRICH\DIRICH5D2\DIRICH5D2.DSN		
Modified:	Wednesday, February 28, 2024	Size: A3	Page: 2 / 9
Designer:	M.Traxler/H.Heggen	Layouter:	H.Kavan

Bank 0,1,4,8: no true LVDS outputs
Bank 0,1,4,8: no true LVDS inputs
Bank 2,3,6,7: LVDS inputs, 50% LVDS outputs



ADC introduces noise to signal inputs and should not be accessed while data is taken whith very low thresholds (highest sensitivity).

Part No.	Resin Color	Forward voltage Vf		Reverse current Ir		Light wavelength Dominant λD		Brightness Iv		
		Typ. (V)	If (mA)	Max. (µA)	Vr (V)	Typ. (nm)	If (mA)	Min. (mcd)	Typ. (mcd)	If (mA)
SML-P11MT	Transparent Colorless	1.9				569		0.63	2.1	
SML-P11YT		1.9				586		2.5	7.6	
SML-P11DT		1.8	1	100	4	605	1	2.5	7.3	1
SML-P11UT		1.8				621		1.6	5.5	
SML-P11VT		1.8				626		1.0	3.6	

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FPGA

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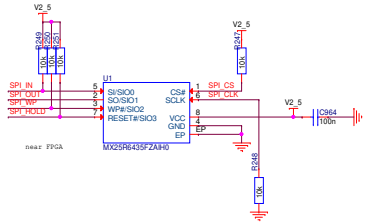
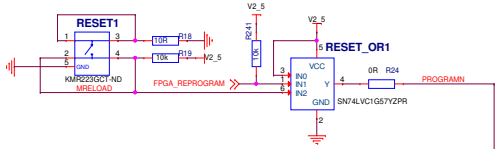
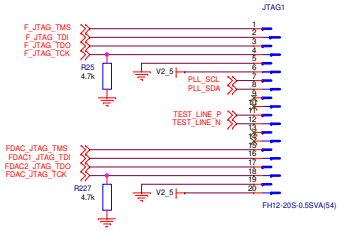
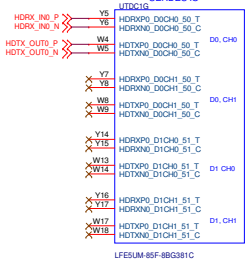
Modified: Wednesday, February 28, 2024 | Size: A2 | Page: 3 / 9
Designer: M.Traxler/U.Hessen | Layouter: H.Kavan

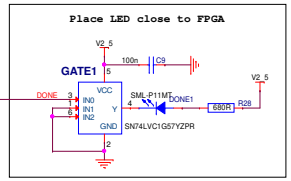


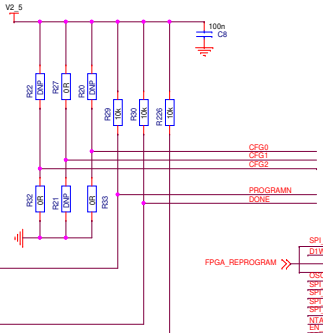


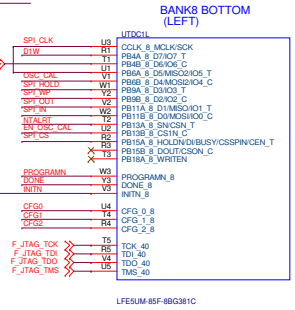




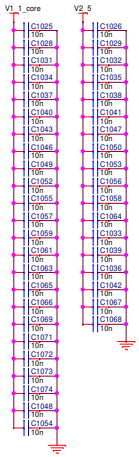
unused serdes channels can be left unpowered and
input signals left floating.
VCCA has always to be powered.



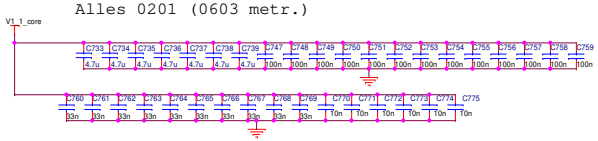


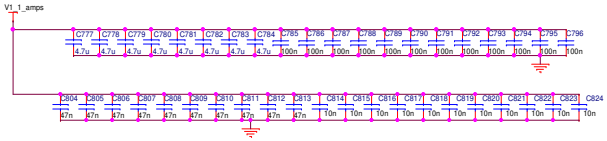


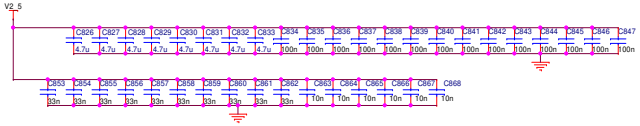
Current return path connections...

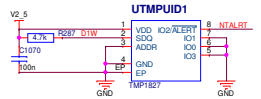


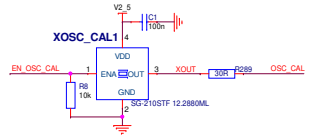
Am Schluß: Gleichmäßig auf dem Board verteilen.
Alles 0201 (0603 metr.)











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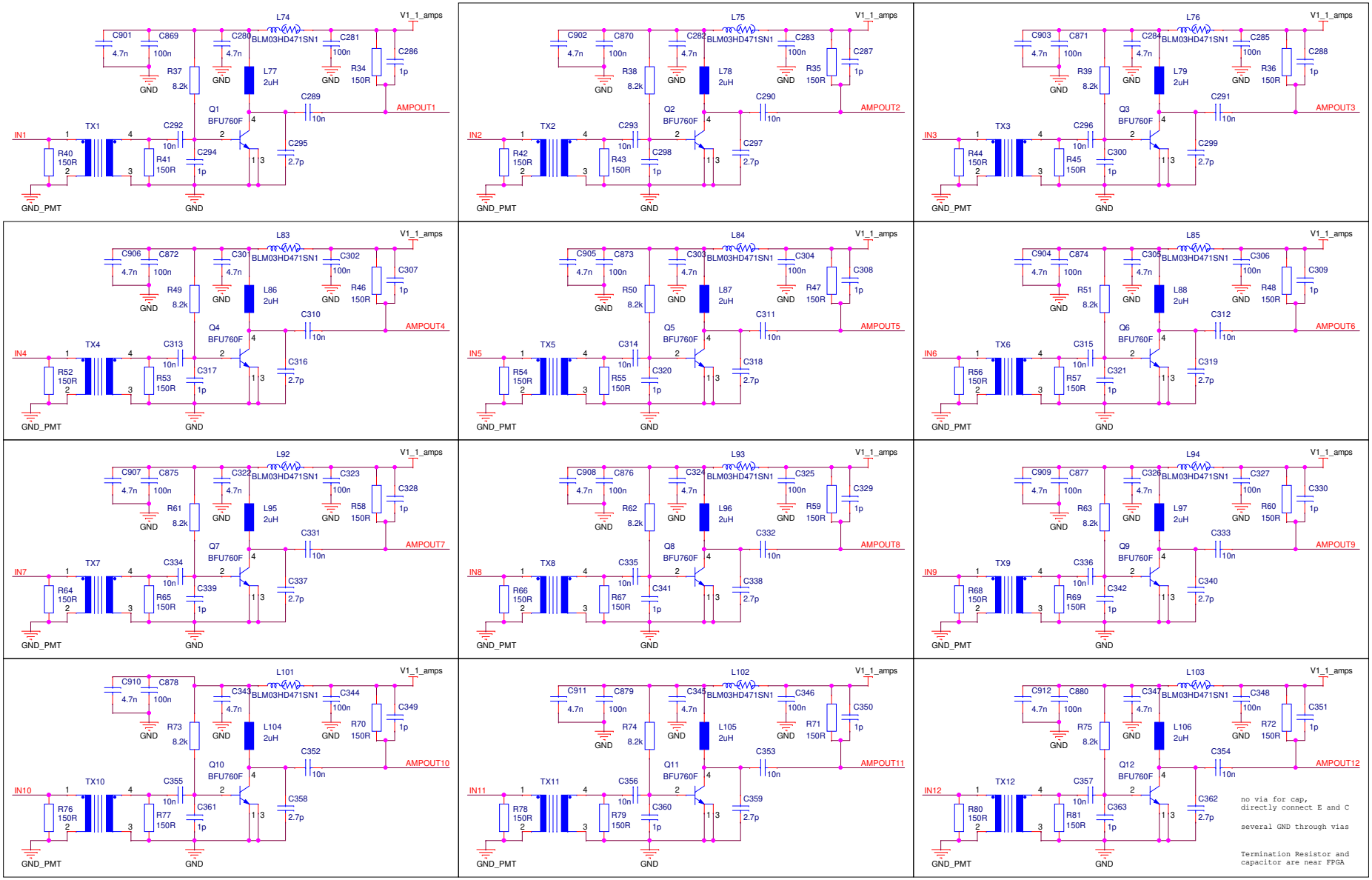
FPGA2

Design: K:\GSU\OBCOME_AND_KISS\DIRICH\DIRICH5D2\DIRICH5D2.DSN
Modified: Wednesday, February 28, 2024
Size: A2
Page: 4 / 9
Designer: M.Traxler/H.Hoeppe
Layouter: H.Kavan



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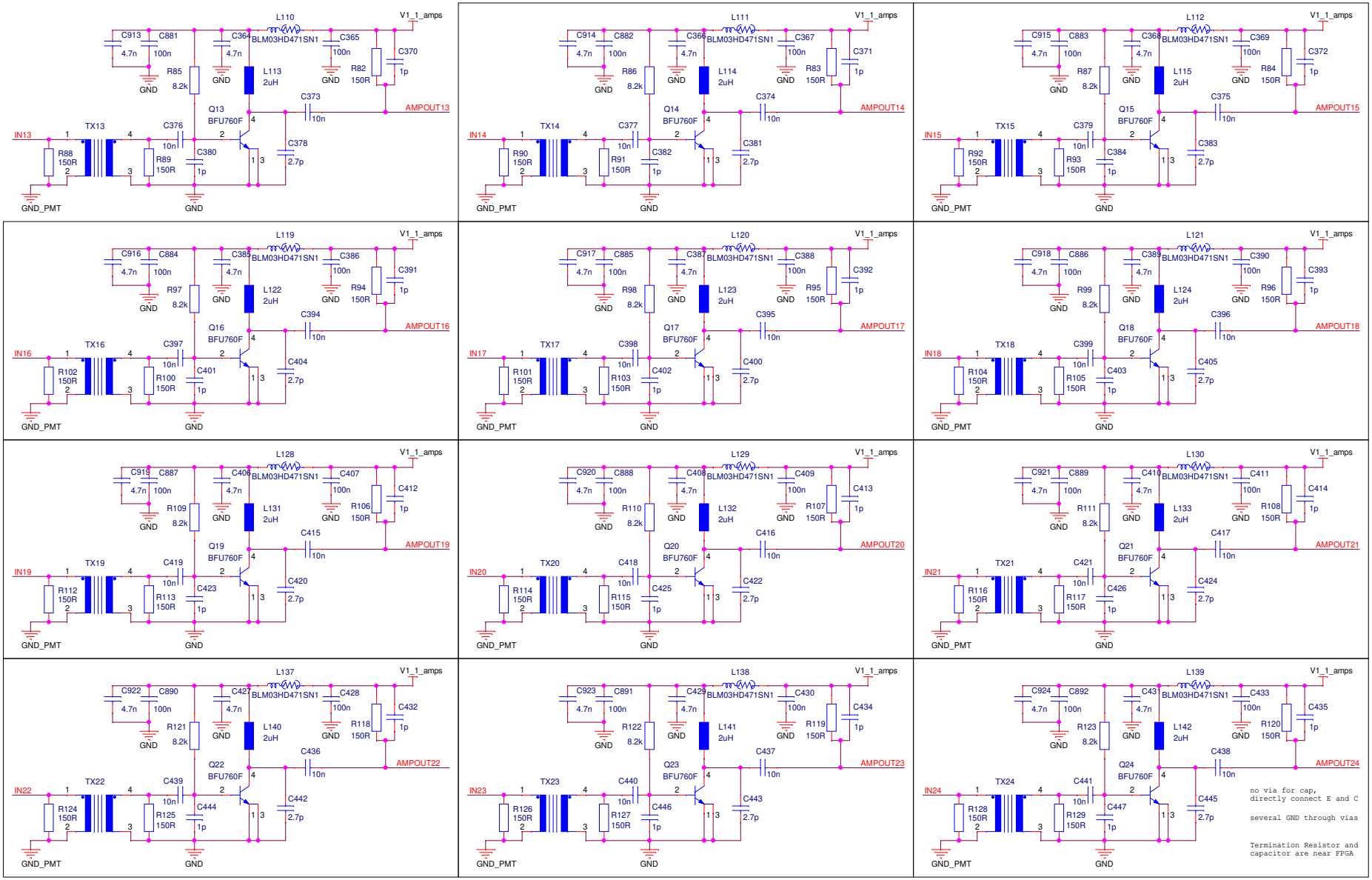
CHANNEL 1-12

Design: K:\GSI\JOB\COME_AND_KISS\DIRICH\DIRICH5D2\DIRICH5D2.DSN
Modified: Wednesday, February 28, 2024
Designer: M.Traxler/H.Heggen
Size: A3
Page: 5 / 9
Layouter: H.Kavan



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CHANNEL 13-24

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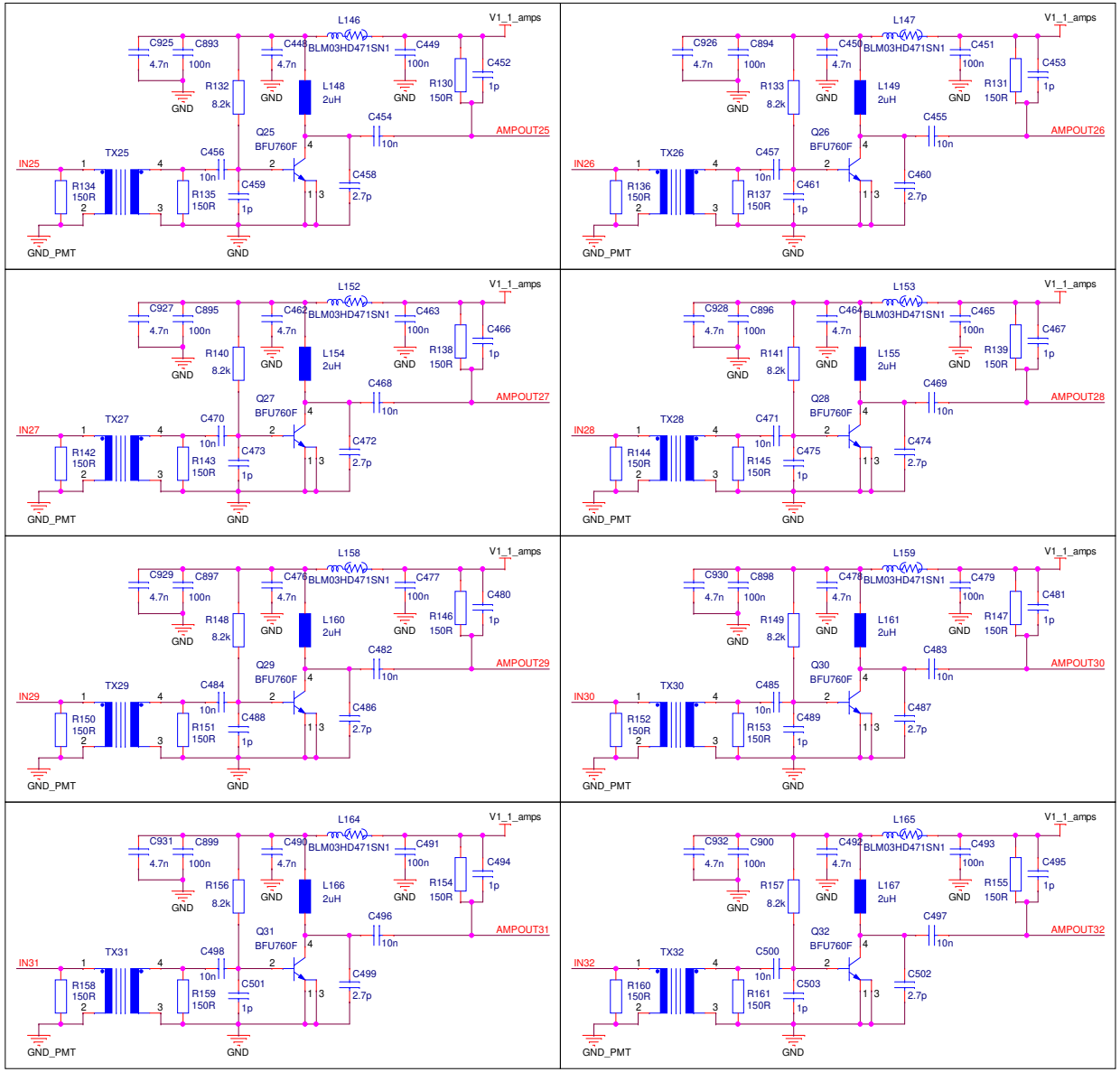
Modified: Wednesday, February 28, 2024
Designer: M.Traxler/H.Heggen
Size: A3
Page: 6 / 9
Layouter: H.Kavan



IN[32..1] IN[32..1]

AMPOUT[32..1] AMPOUT[32..1]

no via for cap,
directly connect E and C

several GND through vias

Termination Resistor and
capacitor are near FPGA

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CHANNEL 25-32

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Modified: Wednesday, February 28, 2024 Size: A3 Page: 7 / 9
Designer: M.Traxler/H.Heggen Layouter: H.Kavan

wire around FPGA, from output side to input side

PWM_IN[32..1] PWM_IN[32..1]

DAC_OUT[32..1] DAC_OUT[32..1]

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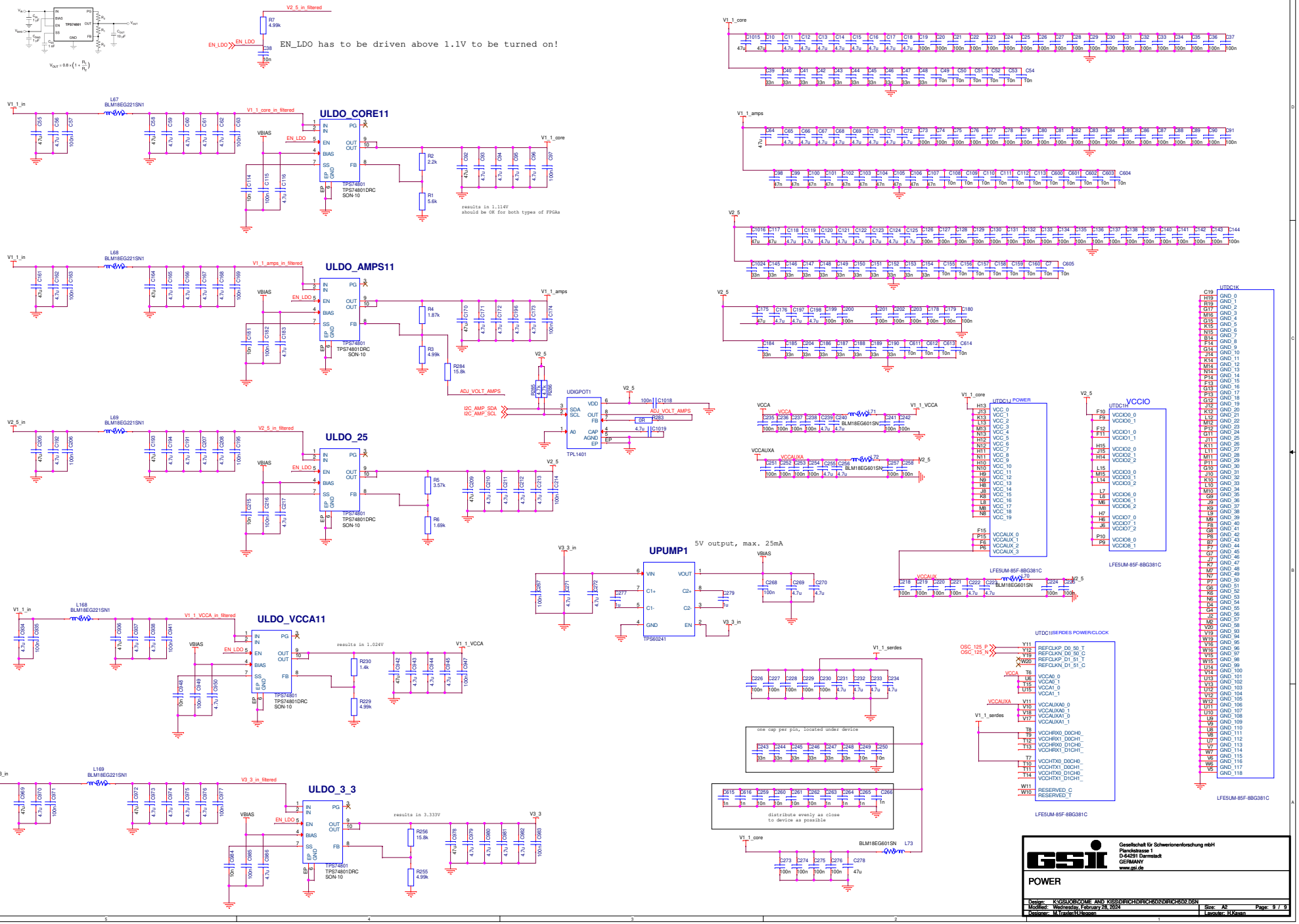
DACs_1-32

Design:	K:\GSI\OB\COME_AND_KISS\DIRICH\DIRICH5D2\DIRICH5D2.DSN		
Modified:	Wednesday, February 28, 2024	Size: A3	Page: 8 / 9
Designer:	M.Traxler/H.Hegner	Layouter:	H.Kavan


EN_LDO has to be driven above 1.1V to be turned on!
ULDO_CORE11
ULDO_AMPS11
ULDO_25
ULDO_VCCA11
ULDO_3_3
UPUMP1
5V output, max. 2.5mA
TPS74801
TPS74801DRC
SON-10
TPL1401
TPS60241
BLM18EG221SN1
BLM18EG601SN
LFE5UM-85F-8BG381C
UTDC1K
UTDC1V
UTDC1J POWER
UTDC1I SERDES POWER/CLOCK
VCCIO
POWER
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Design: K:\GSU\OBCOME_AND_KISS\DIRICH\DIRICH5D2\DIRICH5D2.DSN
Modified: Wednesday, February 28, 2024
Size: A2
Page: 9 / 9
Designer: M.Traxler/H.Hoeppen
Layouter: H.Kavan