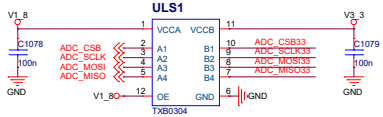
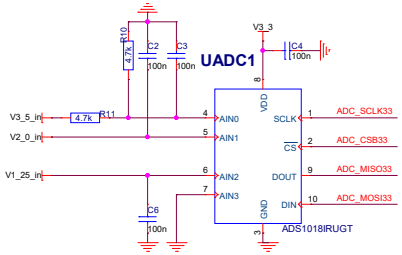
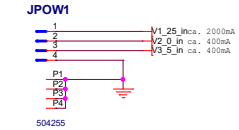
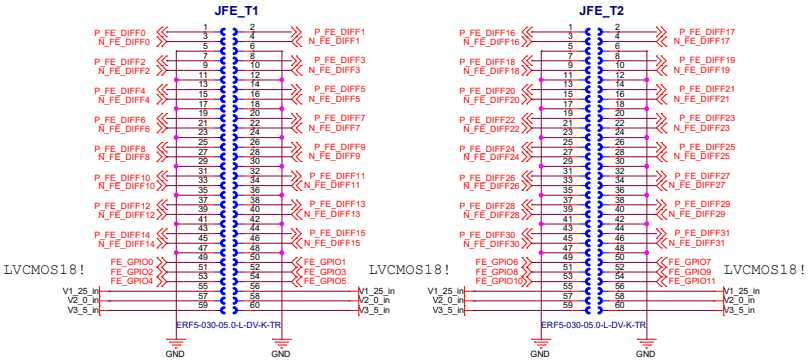
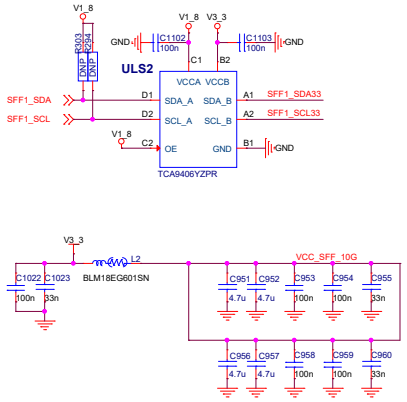


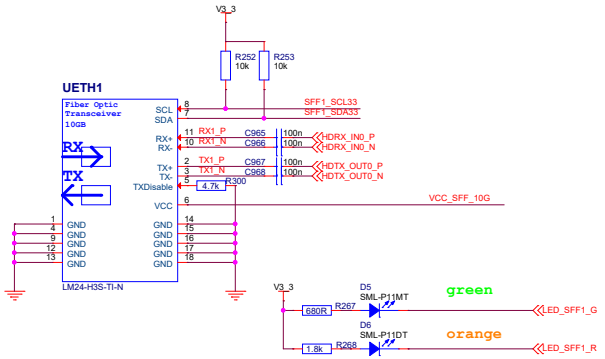


ADC introduces noise to signal inputs and should not be accessed while data is taken whith very low thresholds (highest sensitivity).

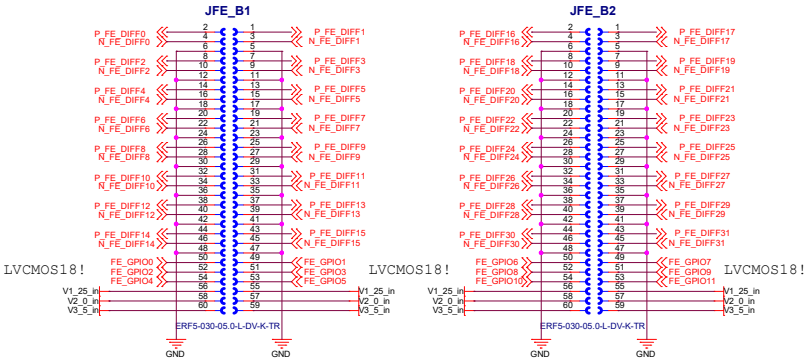


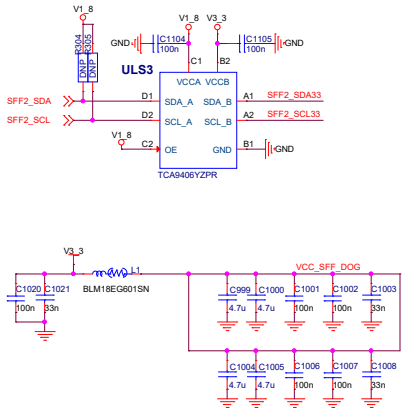


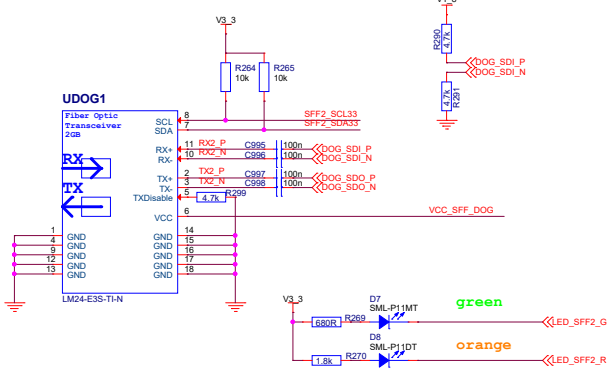




Bridge from ETH RX to DL_SDI?
Any bridge for ETH/DL fusion on one optical cable?







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GERMANY
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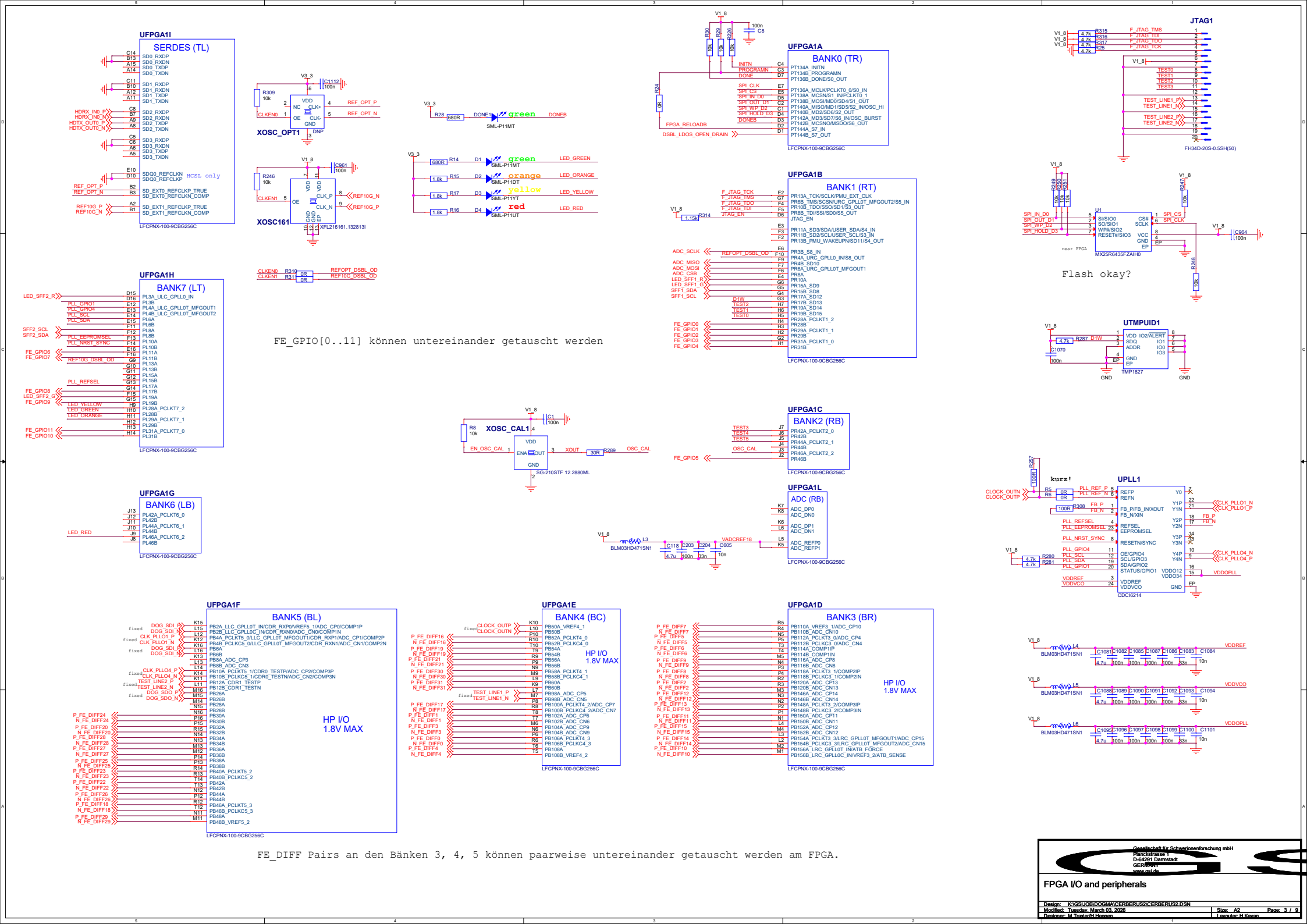
I/O Connectors

Design: K:\GSI\JOB\DOGMA\CERBERUS2\CERBERUS2.DSN
Modified: Tuesday, February 24, 2026
Designer: M.Traxler / H.Hoppen
Size: A2 Page: 1 / 9
Layouter: H.Kavan


UFPGA1I
SERDES (TL)
LFCPNX-100-9CBG256C
XOSC_OPT1
XOSC161
UFPGA1A
BANK0 (TR)
JTAG1
FH34D-20S-0.5SH(50)
UFPGA1B
BANK1 (RT)
Flash okay?
UTMPUID1
TMP1827
UFPGA1H
BANK7 (LT)
FE_GPIO[0..11] können untereinander getauscht werden
XOSC_CAL1
UFPGA1C
BANK2 (RB)
UFPGA1L
ADC (RB)
UFPGA1G
BANK6 (LB)
UPLL1
CDCI6214
UFPGA1F
BANK5 (BL)
HP I/O
1.8V MAX
UFPGA1E
BANK4 (BC)
UFPGA1D
BANK3 (BR)
FE_DIFF Pairs an den Bänken 3, 4, 5 können paarweise untereinander getauscht werden am FPGA.
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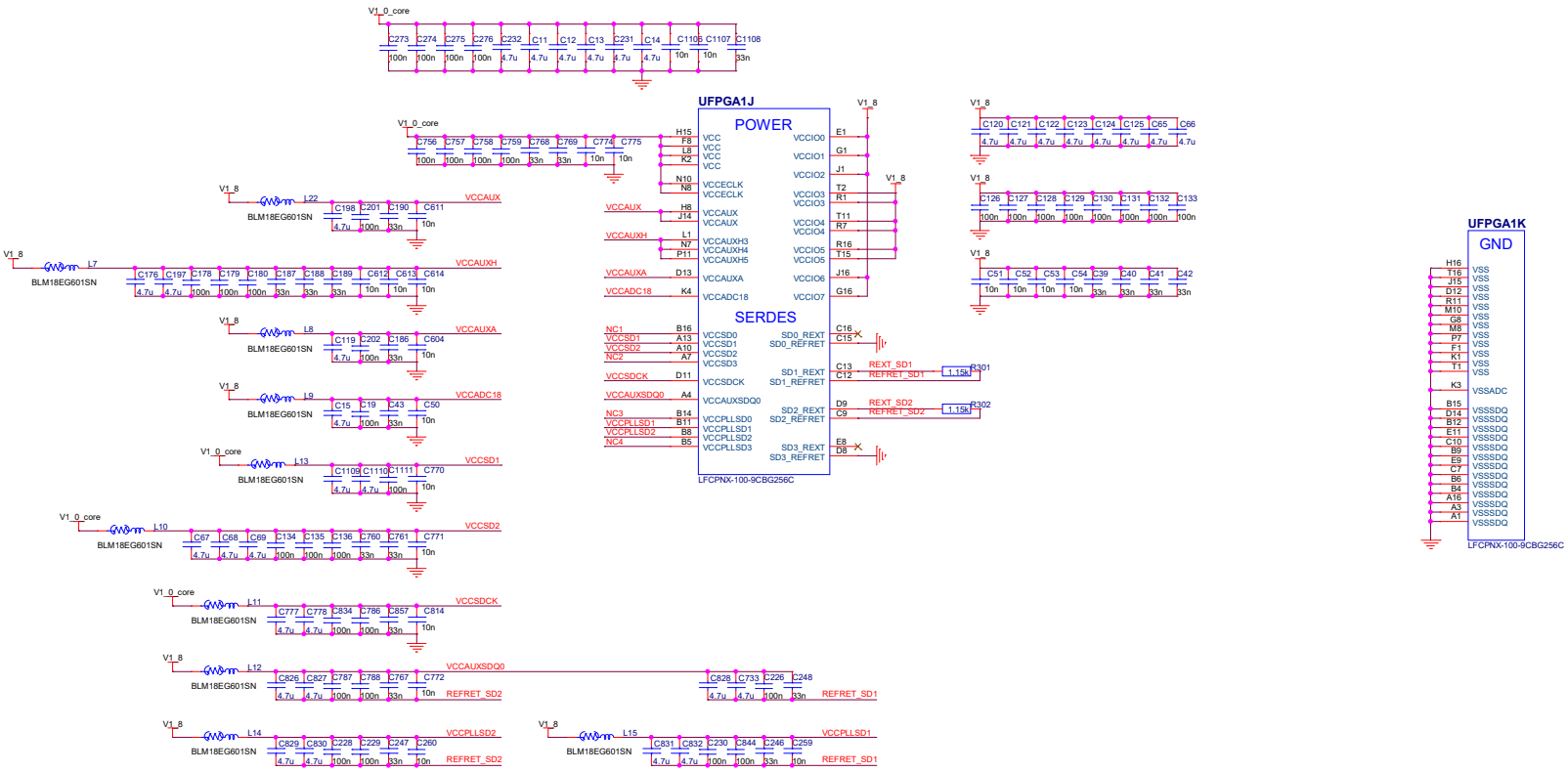
FPGA I/O and peripherals
Design: K:\GSU\OBI\DOG\MAVCERBERUS2\CERBERUS2.DSN
Modified: Tuesday, March 03, 2026
Size: A2
Page: 3 / 9
Designer: M.Traxler/H.Hoenen
Layouter: H.Kavan



Verbesserungen für die nächste Version bzw generell:

- Silkscreen "überall" weglassen, außer bei großen Steckern

- PLL CDCE6214: Externen Zero Delay Mode FB Pfad von OUT2 zu FB_IN (SECREF) routen
- Beide CLKs von EXT PLL an PCLK Pins routen?

- Weiterer GND Pin auf JTAG Header, damit man GND verbinden kann zu Bus Pirate, auch wenn beide JTAG Probes gesteckt sind. Am besten auch neben jeder JTAG Probe einen Pin frei lassen, damit man besser alles gleichzeitig stecken kann.

- LEDS weiter Richtung SFFs schieben?

- Möglichkeit schaffen Sateliten vom FPGA aus zu rebooten? Neu zu flashen?

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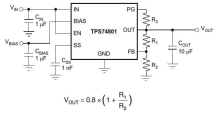
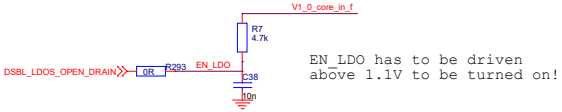
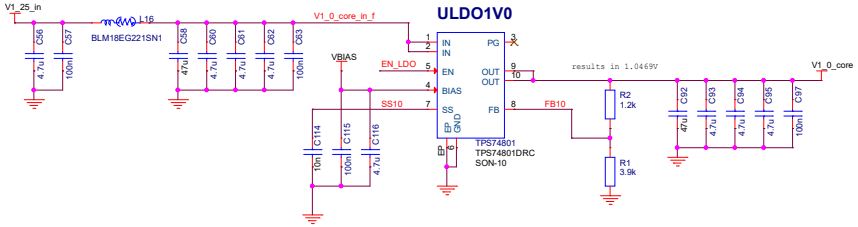
FPGA Power

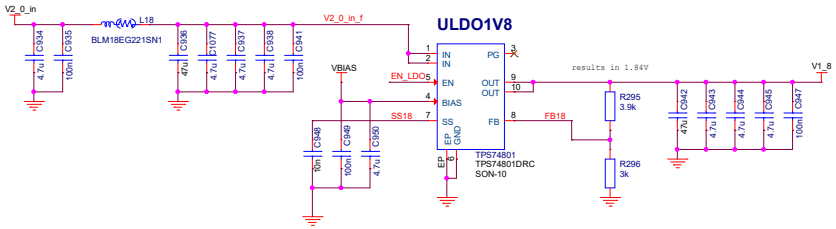
Design:	K:\GSI\JOB\DOGMA\CERBERUS2\CERBERUS2.DSN
Modified: Monday, February 23, 2026	Size: A2 Page: 4 / 9
Designer: M.Traxler/H.Heggen	Layouter: H.Kavan

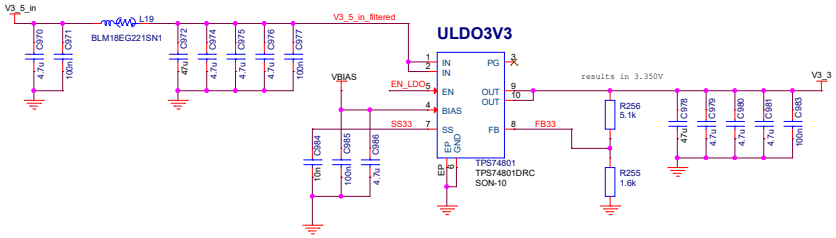




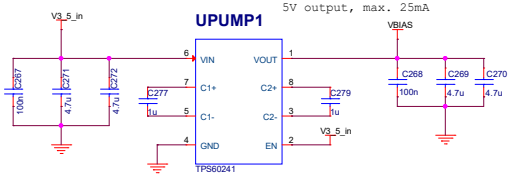
EN_LDO has to be driven
above 1.1V to be turned on!







5V output, max. 25mA



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POWER

Design:	K:\GSI\JOB\DOGMA\CERBERUS2\CERBERUS2.DSN
Modified: Monday, February 23, 2026	Size: A2 Page: 9 / 9
Designer: M.Traxler/H.Heggen	Layouter: H.Kavan