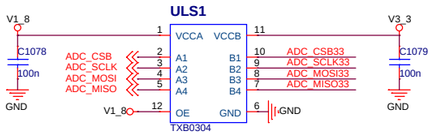
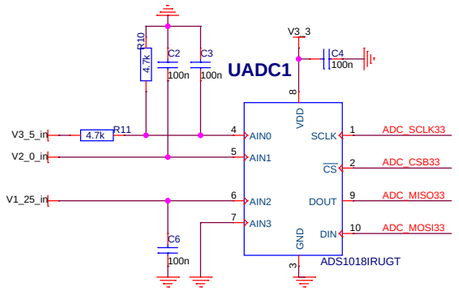
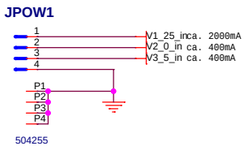
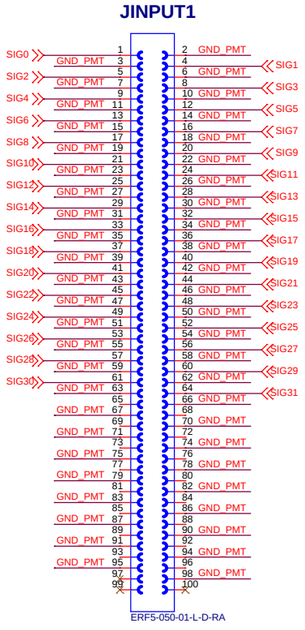
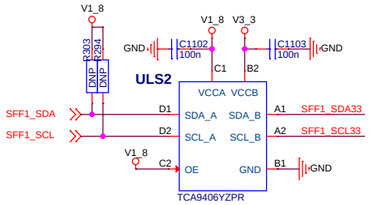


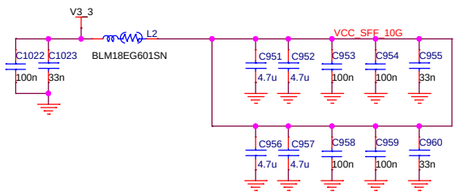


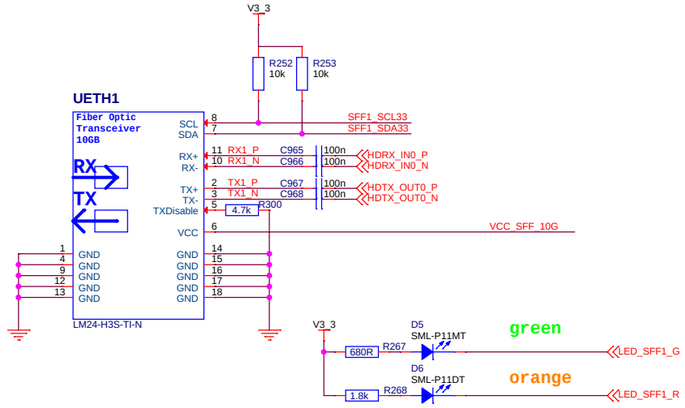


ADC introduces noise to signal inputs and should not be accessed while data is taken whith very low thresholds (highest sensitivity).

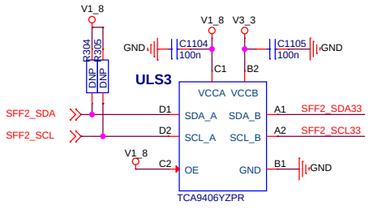


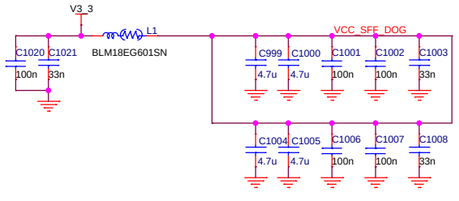


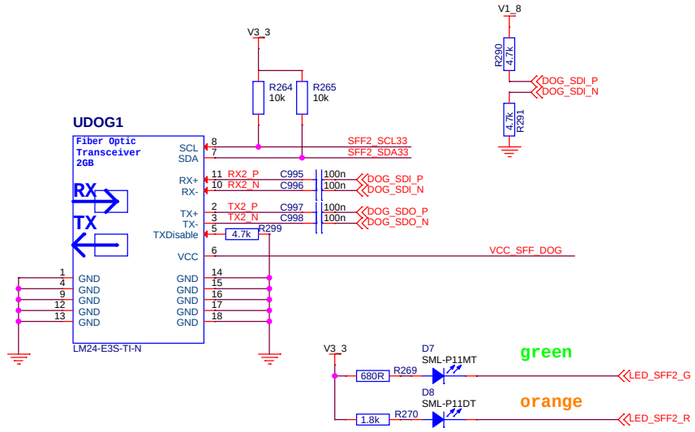




Bridge from ETH RX to DL_SDI?
Any bridge for ETH/DL fusion on one optical cable?







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GERMANY
www.gsi.de

I/O Connectors

Design: K:\GSI\JOB\DOGMA\CERBERUS1\CERBERUS1.DSN
Modified: Monday, January 26, 2026
Size: A2
Page: 1 / 9
Designer: M.Traxler / H. Hoegen
Layouter: H.Kavan

PWM_IN:
these are outputs from this FPGAs point of view....

PWM_IN[31..0] PWM_IN[31..0]

UDAC1-2

PWM_IN6 H9 PB4A_2_CSSPIN_T
PWM_IN12 J8 PB4B_2_C
H8 PB7A_2_T
G7 PB7B_2_C
PWM_IN7 H7 PB9A_2_MCLK/CCLK_T
PWM_IN2 J7 PB9B_2_SO/SPISO_C
H6 PB13A_2_PCLKT2_0_T
H5 PB13B_2_PCLKC2_0_C
PWM_IN3 J5 PB15A_2_T
G4 PB15B_2_C
H4 PB20A_2_PCLKT2_1_T
G3 PB20B_2_PCLKC2_1_C
G2 PB23A_2_T
H3 PB23B_2_C
PWM_IN11 J3 PB24A_2_T
H2 PB24B_2_C
PWM_IN14 J2 PB27A_2_T
G1 PB27B_2_C
PWM_IN15 H1 PB30A_2_SN_T
PWM_IN10 B9 PB30B_2_SI/SISPI_C
C8 PL4A_5_L_GPLLT_IN_T
D8 PL4B_5_L_GPLLC_IN_C
E6 PL5A_5_T
E7 PL7A_5_T
D9 PL7B_5_C
DAC1_CTRL2 E8 PL8C_5_T
F8 PL8D_5_C
F7 PL15A_3_T
F6 PL15B_3_C
DAC1_CTRL3 G9 PL16A_3_T
G8 PL17A_3_PCLKT3_0_T
F5 PL17B_3_PCLKC3_0_C
F4 PL18A_3_T
D7 PL18B_3_C
D6 PT9A_0_T_TLVDS
D5 PT9B_0_C_TLVDS
C6 PT10A_0_T_TLVDS
PWM_IN5 A8 PT10B_0_C_TLVDS
B8 PT11A_0_T_TLVDS
PWM_IN9 A6 PT11B_0_C_TLVDS
B6 PT18A_0_PCLKT0_1_T_TLVDS
E3 PT18B_0_PCLKC0_1_C_TLVDS
D3 PT19A_0_T_TLVDS
A5 PT19B_0_C_TLVDS
DAC1_SCL B5 PT20C_0_SCL/PCLKT0_0_T
DAC1_SDA C3 PT20D_0_SDA/PCLKC0_0_C
PWM_IN8 B4 PT21A_0_T_TLVDS
F2 PT21B_0_C_TLVDS
E2 PT22A_0_T_TLVDS
C2 PT22B_0_C_TLVDS
B3 PT23D_0_PROGRAMN_C
PWM_IN1 A3 PT24A_0_T_TLVDS
F1 PT24B_0_C_TLVDS
DAC1_CTRL1 E1 PT25A_0_T_TLVDS
DAC1_CTRL0 PT25B_0_C_TLVDS
PWM_IN4 A2 PT27A_0_T_TLVDS
B2 PT27B_0_C_TLVDS
PWM_IN0 C1 PT28C_0_INITN_T
PWM_IN13 B1 PT28D_0_DONE_C

V1_8
10k R231
DAC1_RELOAD_OD 0R R306 PROGN1

LCMXO3LF-4300E-5UWG81CTR50

GND

UDAC2-2

PWM_IN28 H9 PB4A_2_CSSPIN_T
PWM_IN18 J8 PB4B_2_C
H8 PB7A_2_T
G7 PB7B_2_C
PWM_IN29 H7 PB9A_2_MCLK/CCLK_T
PWM_IN26 J7 PB9B_2_SO/SPISO_C
H6 PB13A_2_PCLKT2_0_T
H5 PB13B_2_PCLKC2_0_C
PWM_IN24 J5 PB15A_2_T
G4 PB15B_2_C
H4 PB20A_2_PCLKT2_1_T
G3 PB20B_2_PCLKC2_1_C
G2 PB23A_2_T
H3 PB23B_2_C
PWM_IN21 J3 PB24A_2_T
H2 PB24B_2_C
PWM_IN16 J2 PB27A_2_T
For identification of the FPGA G1 PB27B_2_C
PWM_IN22 H1 PB30A_2_SN_T
PWM_IN19 B9 PB30B_2_SI/SISPI_C
C8 PL4A_5_L_GPLLT_IN_T
D8 PL4B_5_L_GPLLC_IN_C
E6 PL5A_5_T
E7 PL7A_5_T
D9 PL7B_5_C
DAC2_CTRL2 E8 PL8C_5_T
F8 PL8D_5_C
F7 PL15A_3_T
F6 PL15B_3_C
DAC2_CTRL3 G9 PL16A_3_T
G8 PL17A_3_PCLKT3_0_T
F5 PL17B_3_PCLKC3_0_C
F4 PL18A_3_T
D7 PL18B_3_C
D6 PT9A_0_T_TLVDS
D5 PT9B_0_C_TLVDS
C6 PT10A_0_T_TLVDS
PWM_IN30 A8 PT10B_0_C_TLVDS
B8 PT11A_0_T_TLVDS
PWM_IN31 A6 PT11B_0_C_TLVDS
B6 PT18A_0_PCLKT0_1_T_TLVDS
E3 PT18B_0_PCLKC0_1_C_TLVDS
D3 PT19A_0_T_TLVDS
A5 PT19B_0_C_TLVDS
DAC2_SCL B5 PT20C_0_SCL/PCLKT0_0_T
DAC2_SDA C3 PT20D_0_SDA/PCLKC0_0_C
PWM_IN25 B4 PT21A_0_T_TLVDS
F2 PT21B_0_C_TLVDS
E2 PT22A_0_T_TLVDS
C2 PT22B_0_C_TLVDS
B3 PT23D_0_PROGRAMN_C
PWM_IN27 A3 PT24A_0_T_TLVDS
F1 PT24B_0_C_TLVDS
DAC2_CTRL1 E1 PT25A_0_T_TLVDS
DAC2_CTRL0 PT25B_0_C_TLVDS
PWM_IN23 A2 PT27A_0_T_TLVDS
B2 PT27B_0_C_TLVDS
PWM_IN20 C1 PT28C_0_INITN_T
PWM_IN17 B1 PT28D_0_DONE_C

V1_8
10k R232
DAC2_RELOAD_OD 0R R307 PROGN2

LCMXO3LF-4300E-5UWG81CTR50

GND

UDAC1-1

GND A1 GND_0
A9 GND_1
E5 GND_2
G5 GND_3
J1 GND_4
J9 GND_5
V1_2_DAC1 C4 VCC_0
D1 VCC_1
F3 VCC_2
E9 VCC_3
V1_8 A4 VCCIO0_0
C5 VCCIO0_1
C7 VCCIO0_2
G6 VCCIO2_0
J4 VCCIO2_1
F9 VCCIO3_0
C9 VCCIO5_0

LCMXO3LF-4300E-5UWG81CTR50

UDAC2-1

GND A1 GND_0
A9 GND_1
E5 GND_2
G5 GND_3
J1 GND_4
J9 GND_5
V1_2_DAC2 C4 VCC_0
D1 VCC_1
F3 VCC_2
E9 VCC_3
V1_8 A4 VCCIO0_0
C5 VCCIO0_1
C7 VCCIO0_2
G6 VCCIO2_0
J4 VCCIO2_1
F9 VCCIO3_0
C9 VCCIO5_0

LCMXO3LF-4300E-5UWG81CTR50

UDAC1-3

DAC_JTAG_CON B7 PT13C_0_TDO_T
FDAC1_JTAG_TDI A7 PT13D_0_TDI_C
FDAC_JTAG_TCK E4 PT15C_0_TCK_T
FDAC_JTAG_TMS D4 PT15D_0_TMS_C
D2 PT23C_0_JTAGENB_T

LCMXO3LF-4300E-5UWG81CTR50

UDAC2-3

FDAC2_JTAG_TDO B7 PT13C_0_TDO_T
A7 PT13D_0_TDI_C
FDAC_JTAG_TCK E4 PT15C_0_TCK_T
FDAC_JTAG_TMS D4 PT15D_0_TMS_C
D2 PT23C_0_JTAGENB_T

LCMXO3LF-4300E-5UWG81CTR50

V1_8

C650 C651 C652 C653 C654 C658 C659 C660 C661 C662 C663 C664 C665 C666 C667 C668 C669
4.7u 4.7u 4.7u 4.7u 4.7u 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n 100n

C677 C678 C679 C680 C681 C682 C683 C684 C685 C686 C687 C688 C689 C690 C693 C694 C695 C696
47n 47n 47n 47n 47n 47n 47n 47n 47n 47n 10n 10n 10n 10n 10n 10n 10n 10n

V1_2_DAC1

C609 C610 C655 C698 C699 C700 C701 C702 C703 C711 C712 C713 C714 C715 C721 C722 C723 C724 C725
4.7u 4.7u 4.7u 100n 100n 100n 100n 100n 100n 47n 47n 47n 47n 47n 10n 10n 10n 10n 10n

V1_2_DAC2

C606 C607 C608 C704 C705 C706 C707 C708 C709 C716 C717 C718 C719 C720 C726 C727 C728 C729 C730
4.7u 4.7u 4.7u 100n 100n 100n 100n 100n 100n 47n 47n 47n 47n 47n 10n 10n 10n 10n 10n

Gesellschaft für Schwerionenforschung mbH
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DAC_FPGA

Design: K:\GSIJOB\DOGMA\CERBERUS1\CERBERUS1.DSN	
Modified: Thursday, February 12, 2026	Size: A3 Page: 2 / 9
Designer: M.Traxler/H.Heggen	Layouter: H.Kayan

UFPGA1I

SERDES (TL)

C14	SD0_RXDP	
B13	SD0_RXDN	
A15	SD0_TXDP	
A14	SD0_TXDN	
C11	SD1_RXDP	
B10	SD1_RXDN	
A12	SD1_TXDP	
A11	SD1_TXDN	
HDRX_IN0_P C8	SD2_RXDP	
HDRX_IN0_N B7	SD2_RXDN	
HDTX_OUT0_P A9	SD2_TXDP	
HDTX_OUT0_N A8	SD2_TXDN	
C5	SD3_RXDP	
C6	SD3_RXDN	
A6	SD3_TXDP	
A5	SD3_TXDN	
E10	SDQ0_REFCLKN	HCSL only
D10	SDQ0_REFCLKP	
REF_OPT_P B2	SD_EXT0_REFCLKP_TRUE	
REF_OPT_N B3	SD_EXT0_REFCLKN_COMP	
REF10G_P A2	SD_EXT1_REFCLKP_TRUE	
REF10G_N B1	SD_EXT1_REFCLKN_COMP	

LFCPNX-100-9CBG256C

V3_3 — C1112 100n — R309 10k — CLKEN0 — XOSC_OPT1 (VDD, NC, CLK+, OE, CLK-, GND, DNP) — REF_OPT_P, REF_OPT_N

V1_8 — C961 100n — R246 10k — CLKEN1 — XOSC161 (VDD, OE, CLK_P, CLK_N, GND, EP) — REF10G_N, REF10G_P — XFL216161.132813I

CLKEN0 R310 0R — REFOPT_DSBL_OD
CLKEN1 R311 0R — REF10G_DSBL_OD

V3_3 — R28 680R — DONE1 — green (SML-P11MT) — DONEB

V3_3 — 680R R14 — D1 green (SML-P11MT) — LED_GREEN
1.8k R15 — D2 orange (SML-P11DT) — LED_ORANGE
1.8k R17 — D3 yellow (SML-P11YT) — LED_YELLOW
1.8k R16 — D4 red (SML-P11UT) — LED_RED

UFPGA1A

BANK0 (TR)

V1_8 — R30 10k, R29 10k, R225 10k — C8 100n

	INITN C4	PT134A_INITN
	PROGRAMN C3	PT134B_PROGRAMN
	DONE D7	PT136B_DONE/S0_OUT
R24 0R	SPI_CLK E7	PT136A_MCLK/PCLKT0_0/S0_IN
	SPI_CS E5	PT138A_MCSN/S1_IN/PCLKT0_1
	SPI_IN_D0 D5	PT138B_MOSI/MD0/SD4/S1_OUT
	SPI_OUT_D1 C2	PT140A_MISO/MD1/SD5/S2_IN/OSC_HI
	SPI_WP_D2 C1	PT140B_MD2/SD6/S2_OUT
	SPI_HOLD_D3 D4	PT142A_MD3/SD7/S6_IN/OSC_BURST
	DONEB D3	PT142B_MCSNO/MSDO/S6_OUT
FPGA_RELOADB	D2	PT144A_S7_IN
DSBL_LDOS_OPEN_DRAIN	D1	PT144B_S7_OUT

LFCPNX-100-9CBG256C

JTAG1

V1_8 — 4.7k R315 F_JTAG_TMS 1; 4.7k R316 F_JTAG_TDI 2; 4.7k R317 F_JTAG_TDO 3; 4.7k R25 F_JTAG_TCK 4; 5

V1_8 — TEST0 7, TEST1 8, TEST2 9, TEST3 10, TEST4 11, TEST5 12

TEST_LINE_N 13, TEST_LINE_P 14; 15, 16, 17, 18, 19, 20

FDAC_JTAG_TMS — C1113 100p — R312 30R — TMS_CON
FDAC_JTAG_TCK — R313 30R — C1114 100p
FDAC1_JTAG_TDI, FDAC2_JTAG_TDO — TCK_CON
R227 4.7k

FH12-20S-0.5SVA(54)

UFPGA1B

BANK1 (RT)

V1_8 — R314 1.15k — JTAG_EN D6

F_JTAG_TCK	E2	PR13A_TCK/SCLK/PMU_EXT_CLK
F_JTAG_TMS	G7	PR6B_TMS/SCSN/URC_GPLL0T_MFGOUT2/S5_IN
F_JTAG_TDO	F4	PR10B_TDO/SSO/SDI/S3_OUT
F_JTAG_TDI	F5	PR8B_TDI/SSI/SDO/S5_OUT
	D6	JTAG_EN
I2C_AMP_SDA	E3	PR11A_SD3/SDA/USER_SDA/S4_IN
I2C_AMP_SCL	F3	PR11B_SD2/SCL/USER_SCL/S3_IN
	F2	PR13B_PMU_WAKEUPN/SD11/S4_OUT
	E6	PR3B_S8_IN
ADC_SCLK	REFOPT_DSBL_OD F10	PR4A_URC_GPLL0_IN/S8_OUT
	F9	PR4B_SD10
ADC_MISO	F7	PR6A_URC_GPLL0T_MFGOUT1
ADC_MOSI	F6	PR8A
ADC_CSB	E4	PR10A
LED_SFF1_R	G6	PR15A_SD9
LED_SFF1_G	G5	PR15B_SD8
SFF1_SDA	G4	PR17A_SD12
SFF1_SCL	G3	PR17B_SD13
D1W	H7	PR19A_SD14
TEST2	H6	PR19B_SD15
TEST1	H5	PR28A_PCLKT1_2
TEST0	H4	PR28B
DAC1_RELOAD_OD	H3	PR29A_PCLKT1_1
DAC1_CTRL0	H2	PR29B
DAC1_CTRL3	G2	PR31A_PCLKT1_0
DAC1_CTRL1	H1	PR31B
DAC1_CTRL2		

LFCPNX-100-9CBG256C

Flash okay?

V1_8 — R249 10k, R250 10k, R251 10k — R247 10k

U1: SPI_IN_D0, SPI_OUT_D1, SPI_WP_D2, SPI_HOLD_D3 — SI/SIO0, SO/SIO1, WP#/SIO2, RESET#/SIO3, CS#, SCLK, VCC, GND, EP — SPI_CS, SPI_CLK

near FPGA — MX25R6435FZAIH0 — C964 100n — R248 10k

UTMPUID1

V1_8 — 4.7k R287 D1W — C1070 100n — VDD, IO2/ALERT, SDQ, IO1, ADDR, IO0, IO3, GND, EP — TMP1827

GND — GND

UFPGA1H

BANK7 (LT)

LED_SFF2_R	D15	PL3A_ULC_GPLL0_IN
DAC2_CTRL0	D16	PL3B
PLL_GPIO1	E12	PL4A_ULC_GPLL0T_MFGOUT1
PLL_GPIO4	E13	PL4B_ULC_GPLL0T_MFGOUT2
PLL_SCL	E14	PL6A
PLL_SDA	E15	PL6B
SFF2_SCL	F11	PL8A
SFF2_SDA	F12	PL8B
PLL_EEPROMSEL	F13	PL10A
PLL_NRST_SYNC	F14	PL10B
	E16	PL11A
DAC2_CTRL3	F16	PL11B
DAC2_CTRL2	G9	PL13A
REF10G_DSBL_OD	G10	PL13B
	G11	PL15A
	G12	PL15B
PLL_REFSEL	G13	PL17A
	G14	PL17B
LED_SFF2_G	F15	PL19A
DAC2_CTRL1	G15	PL19B
	H9	PL28A_PCLKT7_2
	H10	PL28B
LED_RED	H11	PL29A_PCLKT7_1
LED_YELLOW	H12	PL29B
LED_GREEN	H13	PL31A_PCLKT7_0
LED_ORANGE	H14	PL31B

LFCPNX-100-9CBG256C

Signale an den Bänken 1 (außer JTAG), 2, 6 & 7
können im Prinzip beliebig getauscht/ verschoben werden.

UFPGA1C

BANK2 (RB)

V1_8 — R239 8.2k, R240 8.2k

	TEST3 J7	PR42A_PCLKT2_0
	TEST4 J6	PR42B
	TEST5 J5	PR44A_PCLKT2_1
	J4	PR44B
	OSC_CAL J3	PR46A_PCLKT2_2
DAC1_SDA	J2	PR46B
DAC1_SCL		

LFCPNX-100-9CBG256C

UFPGA1L

ADC (RB)

	K7	ADC_DP0
	K8	ADC_DN0
	K6	ADC_DP1
	L6	ADC_DN1
	L5	ADC_REFP0
	K5	ADC_REFP1

LFCPNX-100-9CBG256C

V1_8 — L3 BLM03HD471SN1 — C118 4.7u, C203 100n, C204 33n, C605 10n — VADCREF18

kurz!

R257 100R — CLOCK_OUTN, CLOCK_OUTP — R5 0R, R6 0R — 100R R308 FB_P, FB_N

UPLL1

REFP, REFN — Y0 7; Y1P 22, Y1N 21 — CLK_PLLO1_N, CLK_PLLO1_P
FB_P/FB_IN/XOUT, FB_N/XIN — Y2P 18, Y2N 17 — FB_P, FB_N
REFSEL 4, EEPROMSEL 23 — Y3P 14, Y3N 13
RESETN/SYNC 8 — Y4P 10, Y4N 9 — CLK_PLLO4_N, CLK_PLLO4_P
OE/GPIO4 11, SCL/GPIO3 12, SDA/GPIO2 19, STATUS/GPIO1 20
VDDO12, VDDO34 — 16, 15 — VDDOPLL
VDDREF 3, VDDVCO 24 — VDDREF, VDDVCO, GND, EP

CDCI6214

PLL_REFSEL, PLL_EEPROMSEL, PLL_NRST_SYNC, PLL_GPIO4, PLL_SCL, PLL_SDA, PLL_GPIO1

V1_8 — R280 4.7k, R281 4.7k

UFPGA1G

BANK6 (LB)

V1_8 — R274 8.2k, R275 8.2k

J13	PL42A_PCLKT6_0
J12	PL42B
J11	PL44A_PCLKT6_1
J10	PL44B
J9	PL46A_PCLKT6_2
J8	PL46B

DAC2_SCL, DAC2_SDA

LFCPNX-100-9CBG256C

UFPGA1F

BANK5 (BL)

fixed DOG_SDI_P	K15	PB2A_LLC_GPLL0T_IN/CDR_RXP0/VREF5_1/ADC_CP0/COMP1P
DOG_SDI_N	L15	PB2B_LLC_GPLL0C_IN/CDR_RXN0/ADC_CN0/COMP1N
fixed CLK_PLLO1_P	L12	PB4A_PCLKT5_0/LLC_GPLL0T_MFGOUT1/CDR_RXP1/ADC_CP1/COMP2P
CLK_PLLO1_N	K12	PB4B_PCLKC5_0/LLC_GPLL0T_MFGOUT2/CDR_RXN1/ADC_CN1/COMP2N
fixed DOG_SDI_P	K16	PB6A
DOG_SDI_N	L16	PB6B
	K13	PB8A_ADC_CP3
	L13	PB8B_ADC_CN3
fixed CLK_PLLO4_P	L14	PB10A_PCLKT5_1/CDR0_TESTP/ADC_CP2/COMP3P
CLK_PLLO4_N	K14	PB10B_PCLKC5_1/CDR0_TESTN/ADC_CN2/COMP3N
	K11	PB12A_CDR1_TESTP
	L11	PB12B_CDR1_TESTN
fixed DOG_SDO_P	M16	PB26A
DOG_SDO_N	M15	PB26B
	M14	PB28A
DAC2_RELOAD_OD	N15	PB28B
	N16	PB30A
DAC31 AMP31	P16	PB30B
DAC30 AMP30	P15	PB32A
DAC29 AMP29	R15	PB32B
DAC21 AMP21	N14	PB34A
DAC28 AMP28	N13	PB34B
DAC25 AMP25	M13	PB36A
DAC27 AMP27	M12	PB36B
DAC26 AMP26	P14	PB38A
DAC23 AMP23	P13	PB38B
DAC24 AMP24	R14	PB40A_PCLKT5_2
	R13	PB40B_PCLKC5_2
	T14	PB42A
	T13	PB42B
	N12	PB44A
	P12	PB44B
	R12	PB46A_PCLKT5_3
	T12	PB46B_PCLKC5_3
	N11	PB48A
	M11	PB48B_VREF5_2

HP I/O
1.8V MAX

LFCPNX-100-9CBG256C

DAC[31..0] — DAC[31..0]
AMP[31..0] — AMP[31..0]

UFPGA1E

BANK4 (BC)

fixed CLOCK_OUTP	K10	PB50A_VREF4_1
CLOCK_OUTN	L10	PB50B
DAC19	P10	PB52A_PCLKT4_0
AMP19	R10	PB52B_PCLKC4_0
DAC20	T10	PB54A
AMP20	T9	PB54B
DAC17	R9	PB56A
AMP17	P9	PB56B
DAC18	N9	PB58A_PCLKT4_1
AMP18	M9	PB58B_PCLKC4_1
DAC22	L9	PB60A
AMP22	K9	PB60B
DAC14	L7	PB98A_ADC_CP5
AMP14	M7	PB98B_ADC_CN5
DAC16	P8	PB100A_PCLKT4_2/ADC_CP7
AMP16	R8	PB100B_PCLKC4_2/ADC_CN7
DAC15	T8	PB102A_ADC_CP6
AMP15	T7	PB102B_ADC_CN6
DAC13	M6	PB104A_ADC_CP9
AMP13	N6	PB104B_ADC_CN9
DAC12	P6	PB106A_PCLKT4_3
AMP12	R6	PB106B_PCLKC4_3
DAC11	T6	PB108A
AMP11	T5	PB108B_VREF4_2

HP I/O
1.8V MAX

LFCPNX-100-9CBG256C

UFPGA1D

BANK3 (BR)

DAC10	R5	PB110A_VREF3_1/ADC_CP10
AMP10	R4	PB110B_ADC_CN10
DAC9	N5	PB112A_PCLKT3_0/ADC_CP4
AMP9	P5	PB112B_PCLKC3_0/ADC_CN4
DAC7	T3	PB114A_COMP1IP
AMP7	T4	PB114B_COMP1IN
fixed TEST_LINE_P	M5	PB116A_ADC_CP8
TEST_LINE_N	N4	PB116B_ADC_CN8
DAC8	P3	PB118A_PCLKT3_1/COMP2IP
AMP8	P4	PB118B_PCLKC3_1/COMP2IN
DAC6	R2	PB120A_ADC_CP13
AMP6	R3	PB120B_ADC_CN13
DAC4	M3	PB146A_ADC_CP14
AMP4	N3	PB146B_ADC_CN14
DAC3	N2	PB148A_PCLKT3_2/COMP3IP
AMP3	P2	PB148B_PCLKC3_2/COMP3IN
DAC2	P1	PB150A_ADC_CP11
AMP2	N1	PB150B_ADC_CN11
DAC5	L4	PB152A_ADC_CP12
AMP5	M4	PB152B_ADC_CN12
DAC0	L3	PB154A_PCLKT3_3/LRC_GPLL0T_MFGOUT1/ADC_CP15
AMP0	L2	PB154B_PCLKC3_3/LRC_GPLL0T_MFGOUT2/ADC_CN15
DAC1	M2	PB156A_LRC_GPLL0T_IN/ATB_FORCE
AMP1	M1	PB156B_LRC_GPLL0C_IN/VREF3_2/ATB_SENSE

HP I/O
1.8V MAX

LFCPNX-100-9CBG256C

V1_8 — L4 BLM03HD471SN1 — C1081 4.7u, C1082 100n, C1085 100n, C1087 100n, C1086 100n, C1083 33n, C1084 10n — VDDREF

V1_8 — L5 BLM03HD471SN1 — C1088 4.7u, C1089 100n, C1090 100n, C1091 100n, C1092 100n, C1093 33n, C1094 10n — VDDVCO

V1_8 — L6 BLM03HD471SN1 — C1095 4.7u, C1096 100n, C1097 100n, C1098 100n, C1099 100n, C1100 33n, C1101 10n — VDDOPLL

V1_8 — C1 100n — R8 10k — XOSC_CAL1 (VDD, ENA, OUT, GND) — EN_OSC_CAL — XOUT — R289 30R — OSC_CAL
SG-210STF 12.2880ML

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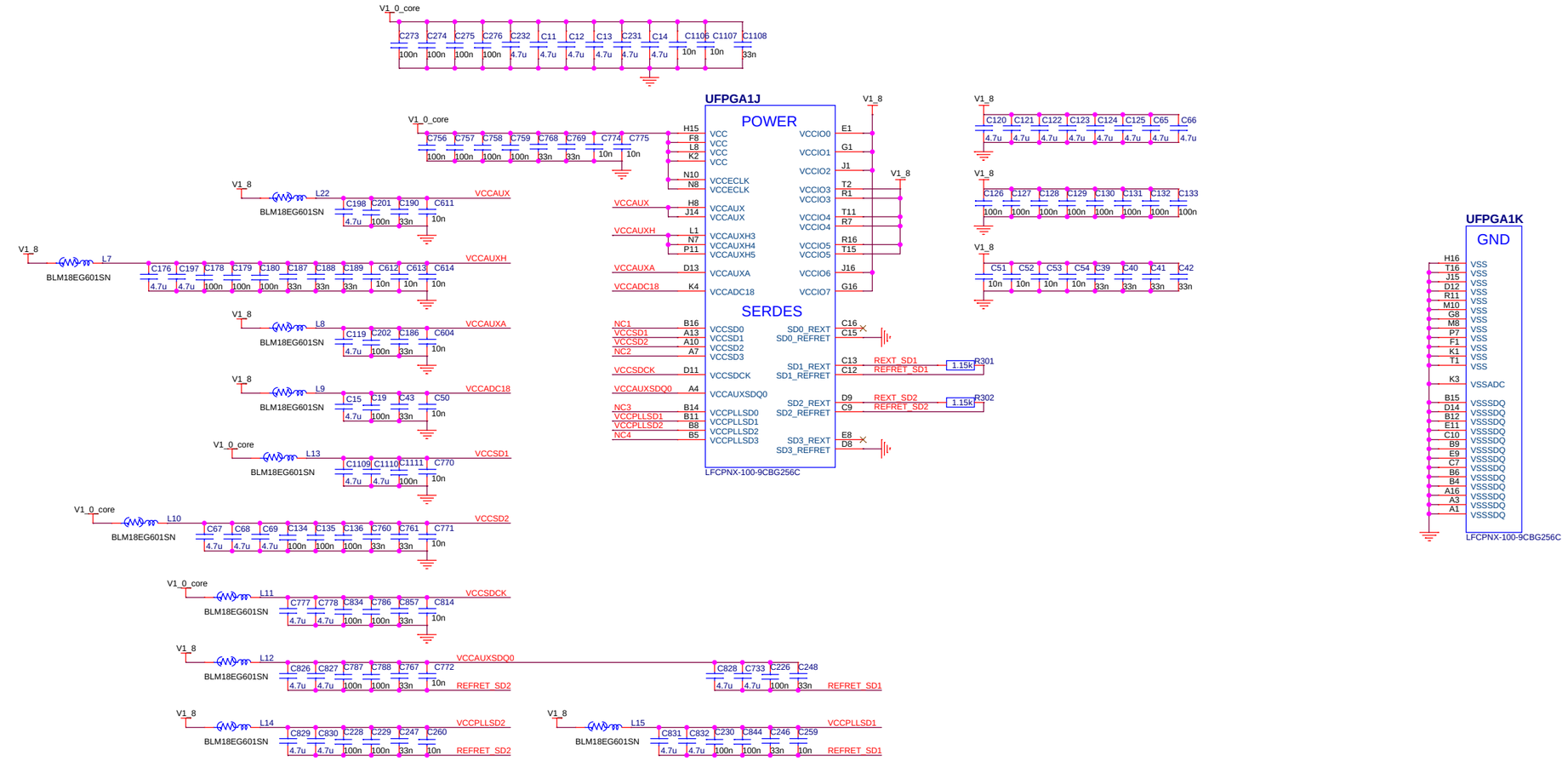
FPGA I/O and peripherals

Design: K:\GSI\JOB\DOGMA\CERBERUS1\CERBERUS1.DSN
Modified: Thursday, February 12, 2026 — Size: A2 — Page: 3 / 9
Designer: M.Traxler/H.Heggen — Layouter: H.Kavan



Verbesserungen für die nächste Version bzw generell:

- **Silkscreen "überall" weglassen, außer bei großen Steckern**
- **PLL CDCE6214: Externen Zero Delay Mode FB Pfad von OUT2 zu FB_IN (SECREF) routen**
- **Beide CLKs von EXT PLL an PCLK Pins routen?**
- **Weiterer GND Pin auf JTAG Header, damit man GND verbinden kann zu Bus Pirate, auch wenn beide JTAG Probes gesteckt sind. Am besten auch neben jeder JTAG Probe einen Pin frei lassen, damit man besser alles gleichzeitig stecken kann.**
- **LEDS weiter Richtung SFFs schieben?**
- **Möglichkeit schaffen Sateliten vom FPGA aus zu rebooten? Neu zu flashen?**

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FPGA Power

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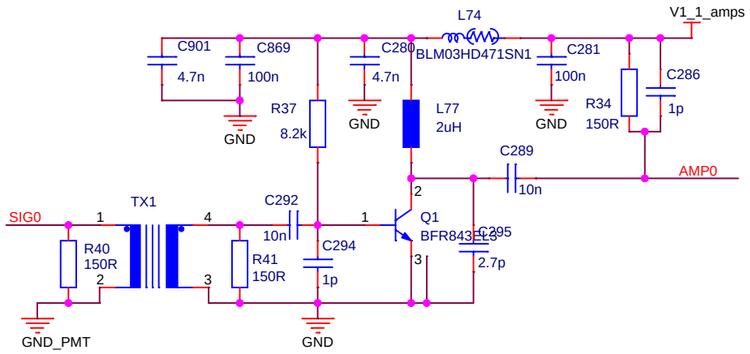
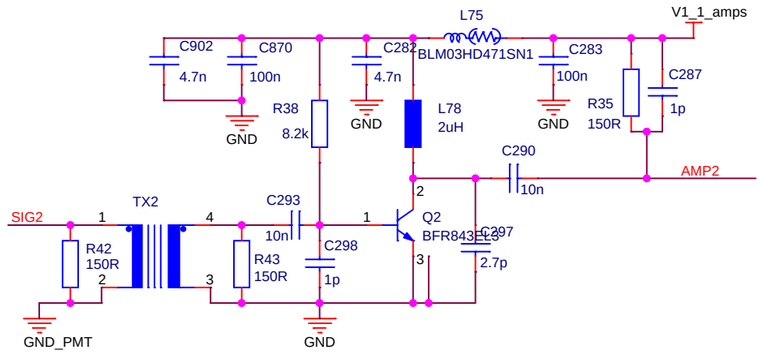
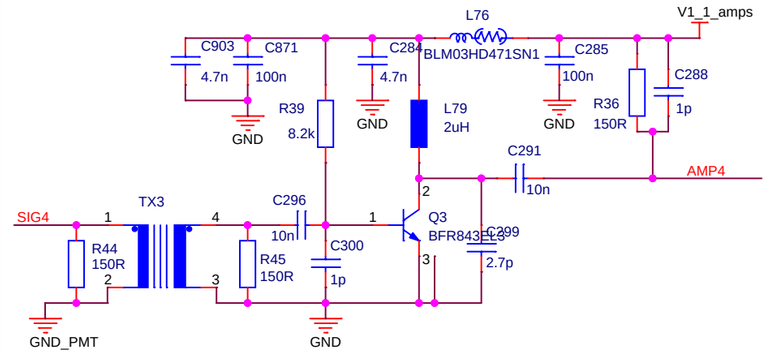
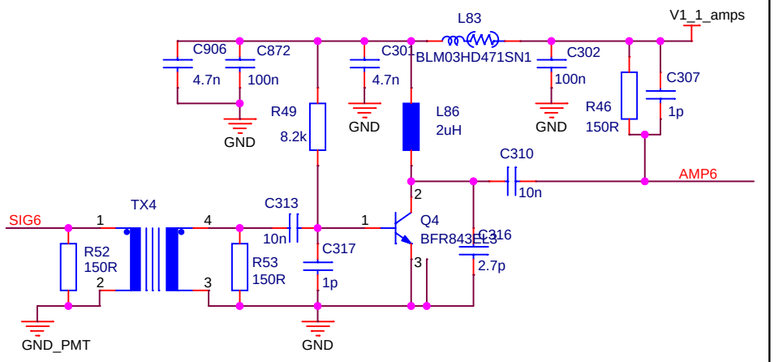
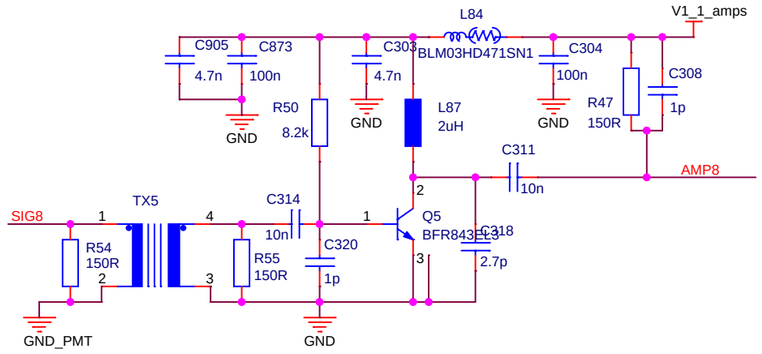
Modified: Thursday, February 12, 2026
Designer: M.Traxler/H.Heggen
Size: A2 Page: 4 / 9
Layouter: H.Kavan

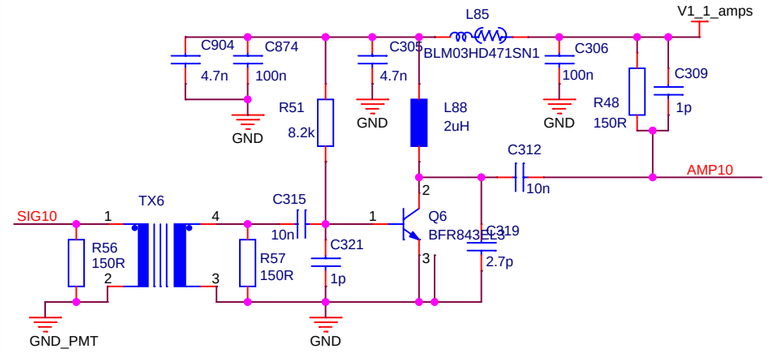


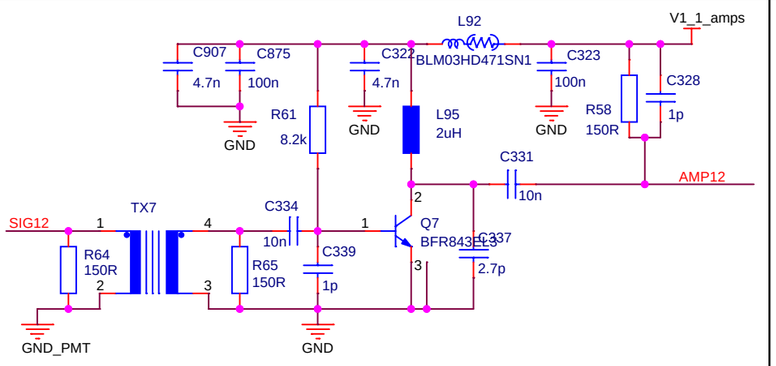


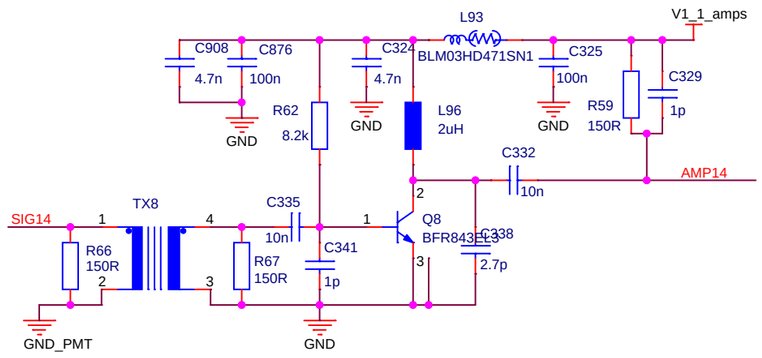


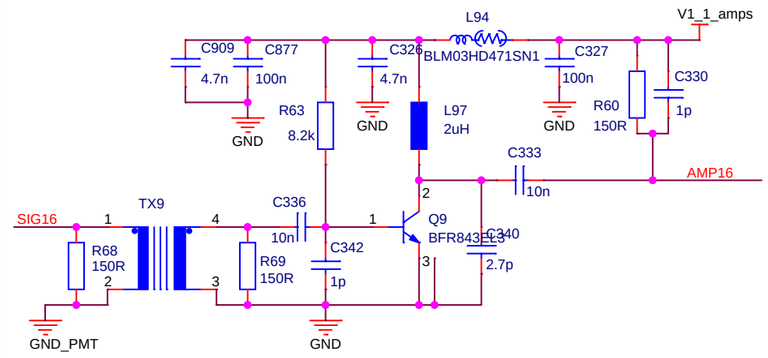


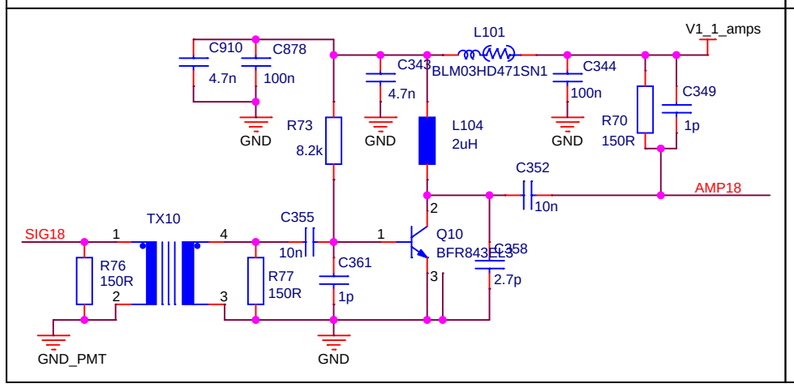


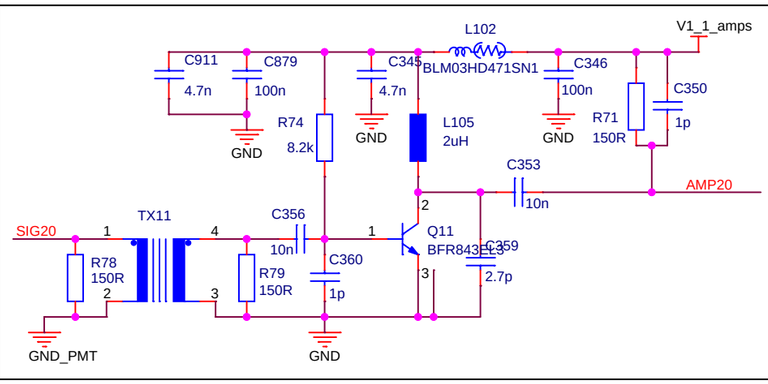


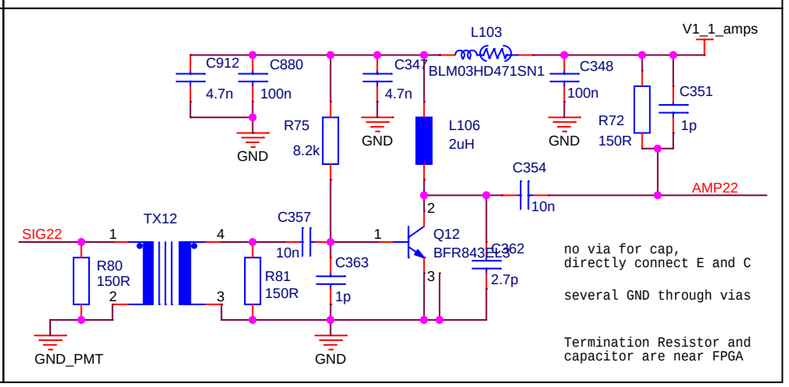












SIG[31..0] SIG[31..0]

AMP[31..0] AMP[31..0]

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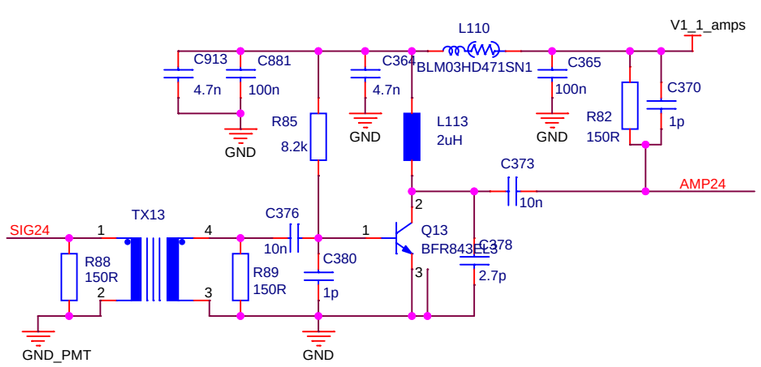
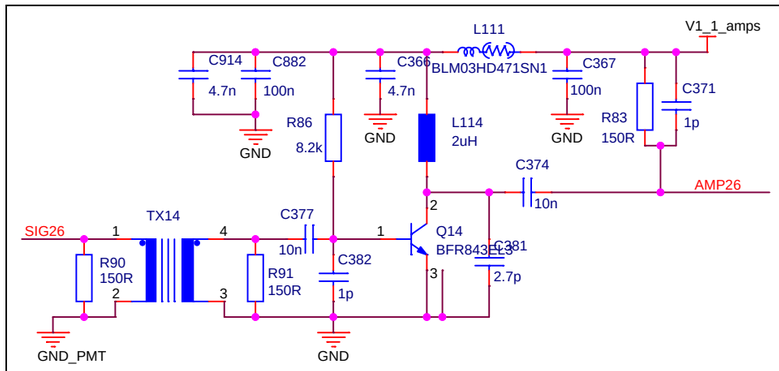
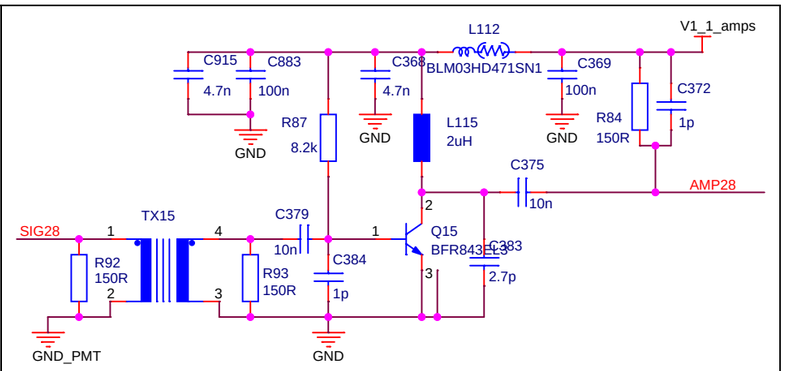
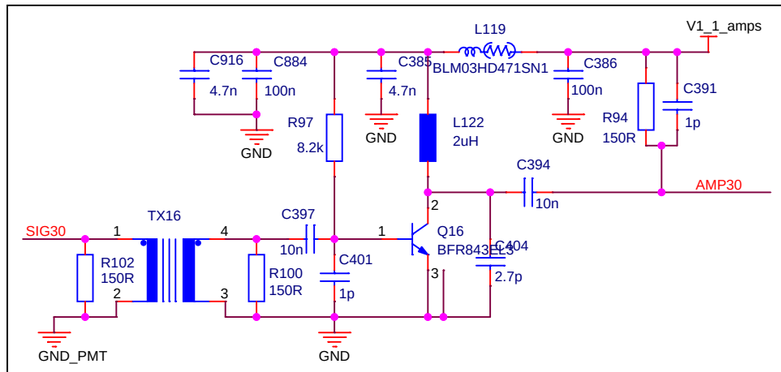
AMPLIFIERS 1

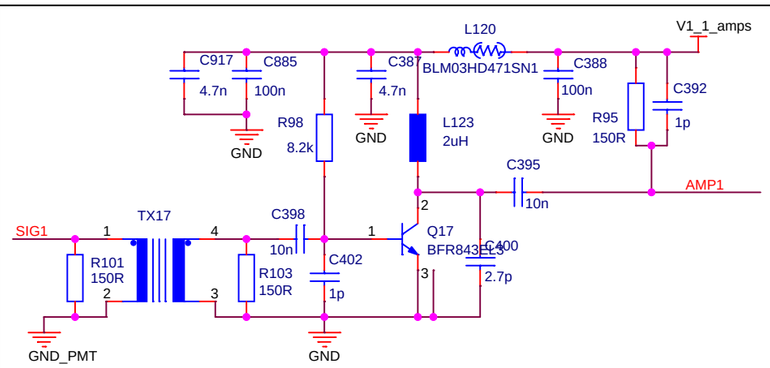
Design:	K:\GSIJOB\DOGMA\CERBERUS1\CERBERUS1.DSN		
Modified:	Thursday, February 12, 2026	Size: A3	Page: 5 / 9
Designer:	M.Traxler/H.Heggen	Layouter:	H.Kavan

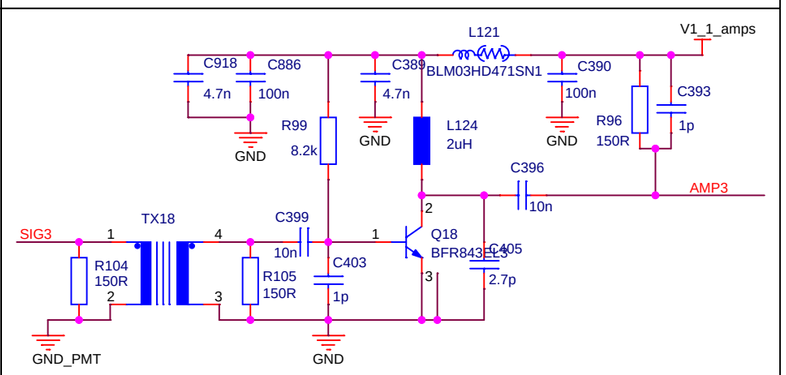


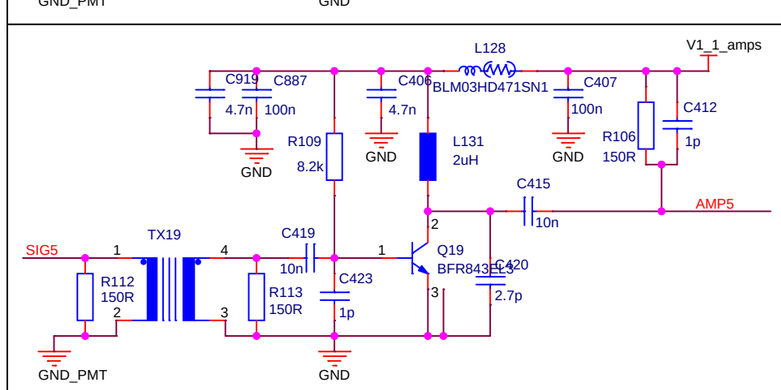


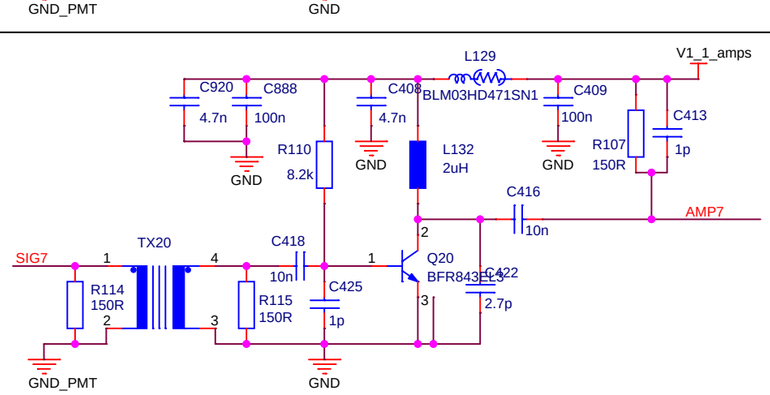


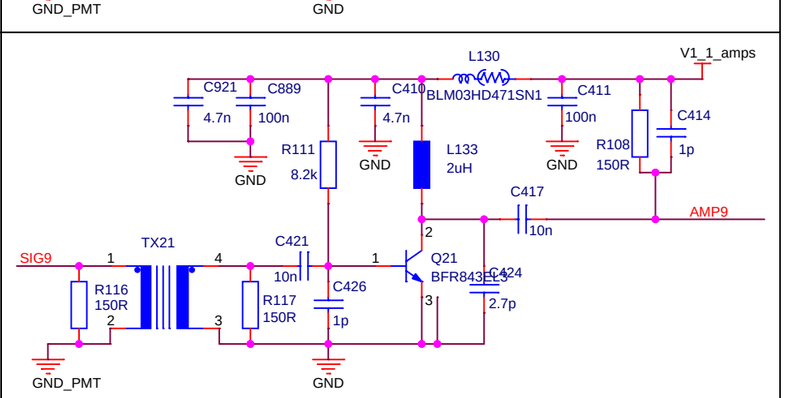


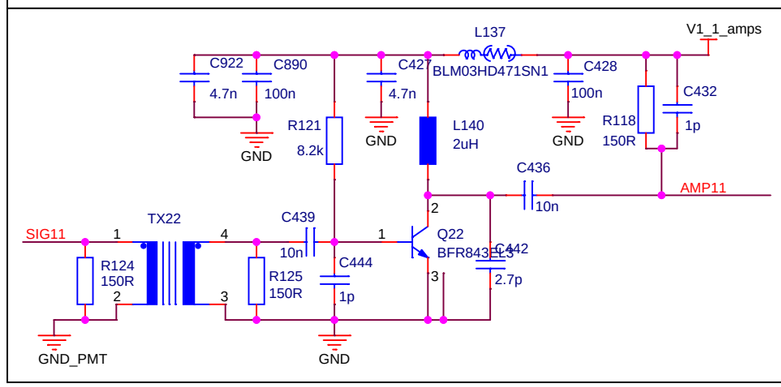


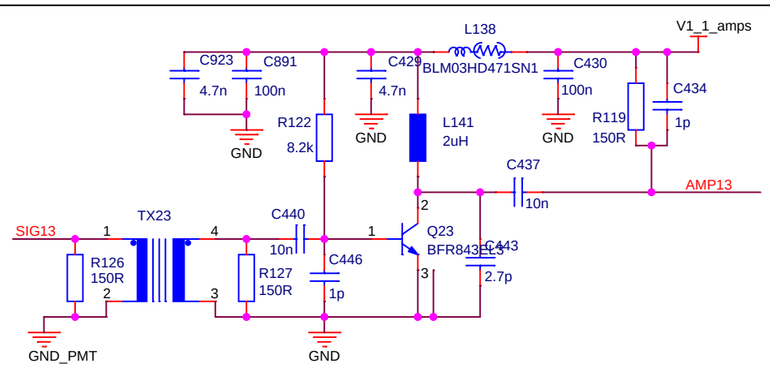


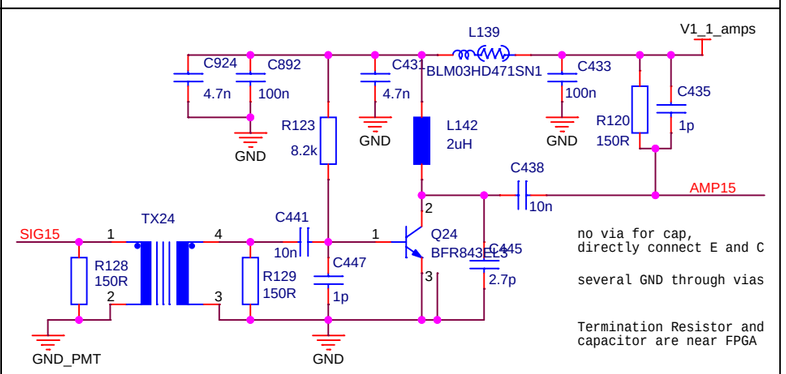












SIG[31..0] SIG[31..0]

AMP[31..0] AMP[31..0]

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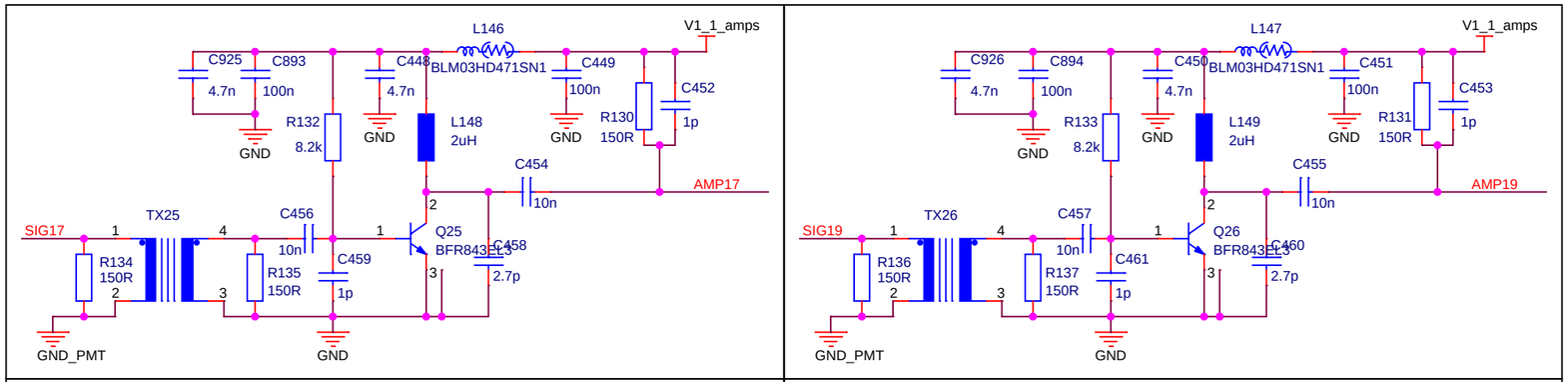
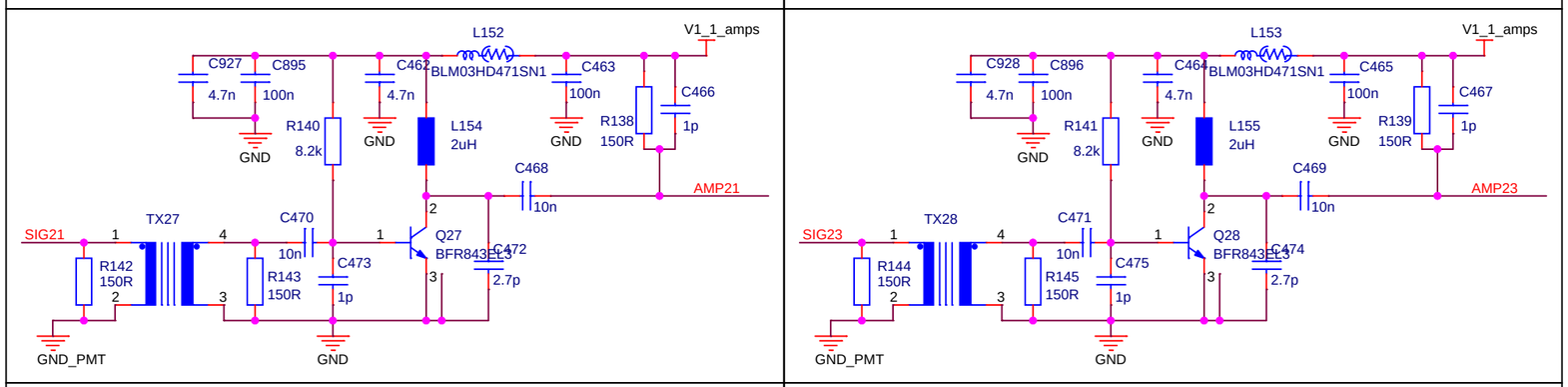
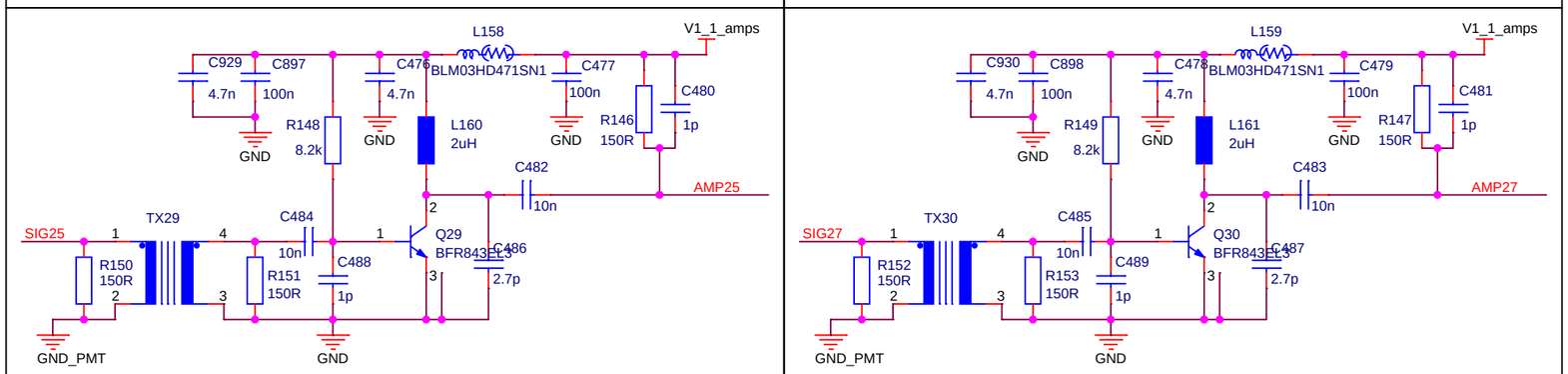
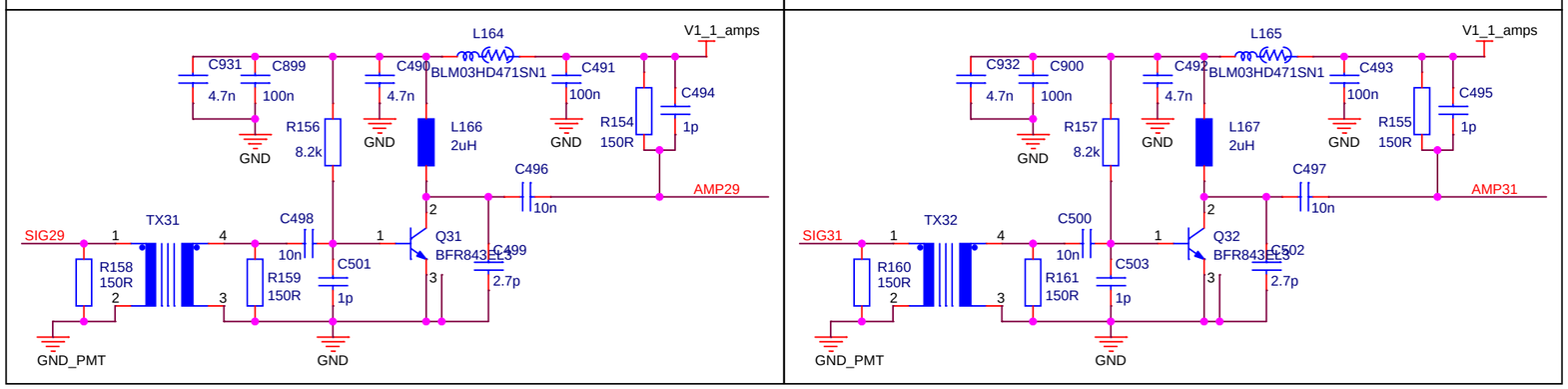
AMPLIFIERS 2

Design: K:\GSIJOB\DOGMA\CERBERUS1\CERBERUS1.DSN		
Modified: Thursday, February 12, 2026	Size: A3	Page: 6 / 9
Designer: M.Traxler/H.Heggen	Layouter: H.Kavan	









no via for cap,
directly connect E and C

several GND through vias

Termination Resistor and
capacitor are near FPGA

SIG[31..0] SIG[31..0]

AMP[31..0] AMP[31..0]

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AMPLIFIERS 3

Design:	K:\GSIJOB\DOGMA\CERBERUS1\CERBERUS1.DSN	
Modified:	Thursday, February 12, 2026	Size: A3 Page: 7 / 9
Designer:	M.Traxler/H.Heggen	Layouter: H.Kayan

wire around FPGA, from output side to input side

PWM_IN[31..0] ⟸ PWM_IN[31..0]

DAC[31..0] ⟹ DAC[31..0]

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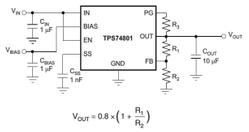
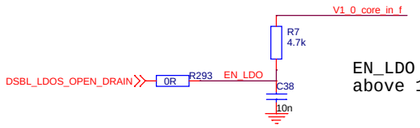
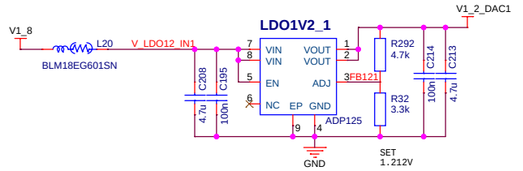
DACs_1-32

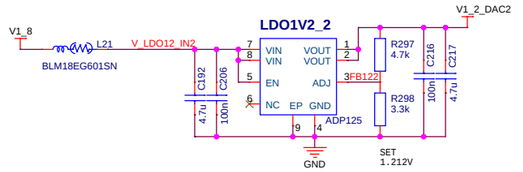
Design: K:\GSI\JOB\DOGMA\CERBERUS1\CERBERUS1.DSN		
Modified: Thursday, February 12, 2026	Size: A3	Page: 8 / 9
Designer: M.Traxler/H.Heggen	Layouter: H.Kayan	

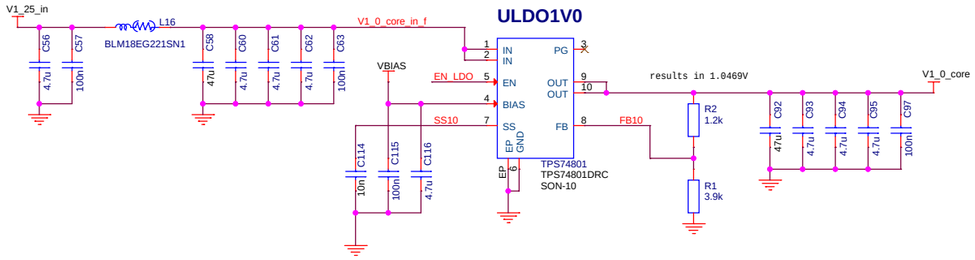


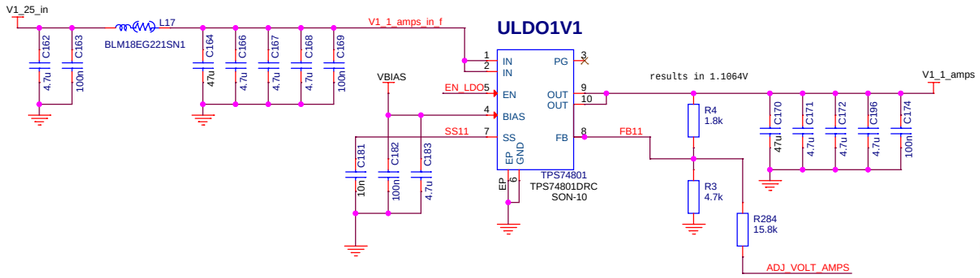


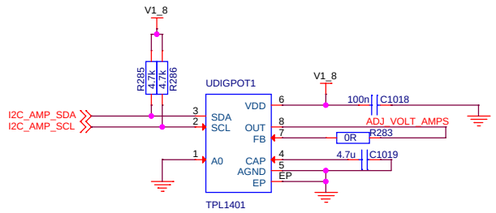
EN_LDO has to be driven
above 1.1V to be turned on!

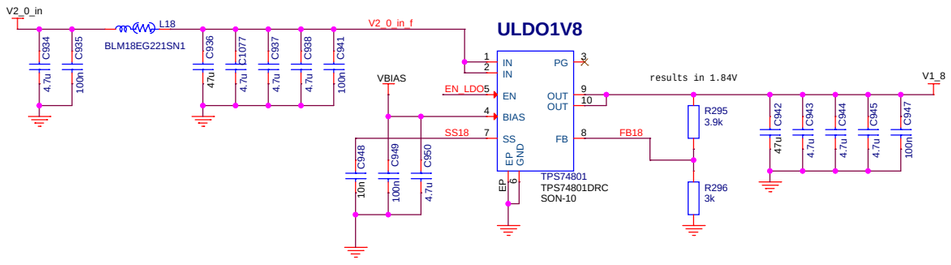


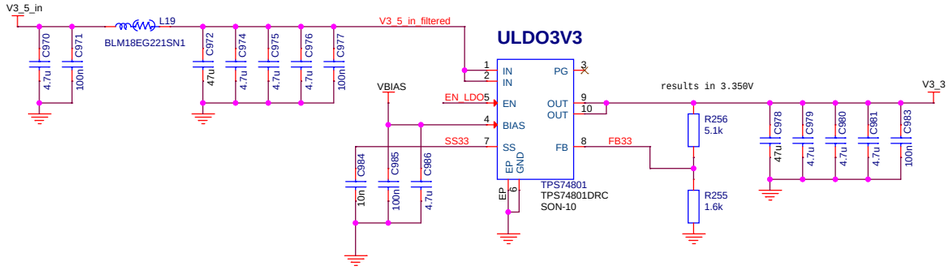




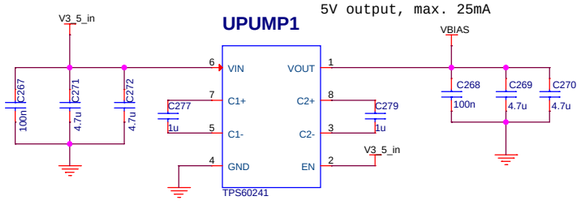








5V output, max. 25mA



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POWER

Design:	K:\GSI\JOB\DOGMA\CERBERUS1\CERBERUS1.DSN
Modified:	Thursday, February 12, 2026
Designer:	M.Traxler/H.Hegger
Size:	A2
Page:	9 / 9
Layouter:	H.Kayan